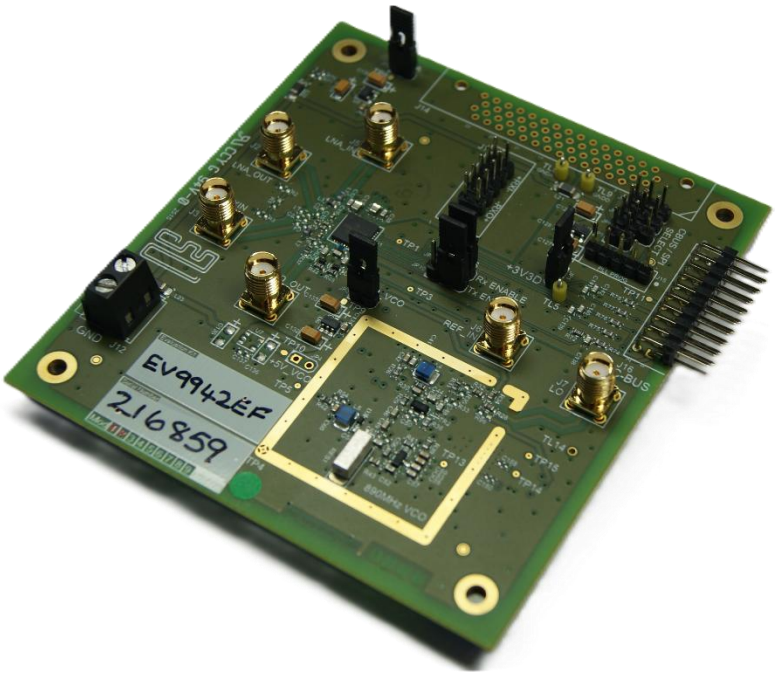
EV9942EF
Evaluation Kit for CMX994EF

UM9942EF/1.0 April 2026 **USER MANUAL** Provisional

Features

- **CMX994EF Evaluation**
- **Receiver:**
  - **LNA**
  - **I/Q Output**
  - **Selectable Filters**
- **Transmit LO Output**
- **Integer-N PLL**
- **19.2 MHz VCTCXO**
- **Flexible External VCO on PCB**
- **On-board Voltage Regulators**
- **PC Control Interface Available**
- **Interfaces to PE0601, EV9810 or EV9100 Evaluation Kits**
- **448 MHz Default Operation**
- **100 MHz to 1000 MHz**



1. Brief Description

The EV9942EF allows the user to investigate all aspects of the CMX994EF integrated circuit, which implements a high-performance direct conversion receiver. The evaluation kit also includes additional circuits that may be used to evaluate system performance, a high-frequency VCO and an optional Fractional-N PLL.

Access is provided to all CMX994EF RF, baseband and control signals by either connector or test points. Test access points are available to accept common test equipment's, such as RF and baseband signal generators and spectrum analysers. All signal paths are matched by suitable components. The overall frequency range of this evaluation kit is for RF frequencies between 100 MHz and 1000 MHz, with default operation at 448 MHz.

The CMX994EF is controlled via its C-BUS serial interface. The PE0003 Interface Card is available separately to support PC-based control of the EV9942EF. The PE0003 uses **ES9942EFxx.exe** PC software, part of the **ES9942EFxx.zip** file, which is available from the CML website.

CONTENTS

1. Brief Description 1
2. History 4
2.1. Glossary 4

3. EV9942EF System Block Diagram 5

4. Preliminary Information 6
4.1. Laboratory Equipment 6
4.2. Power Supply 6
4.3. Handling Precautions 6
4.3.1. Static Protection 6
4.3.2. Contents - Unpacking 6
4.3.3. Approvals 6

5. Quick Start 7
5.1. First – Initial Setup 7
5.1.1. Make External Connections and Apply Power 7
5.1.2. Hardware/Software Installation (for PE0003) 8
5.2. Second – Configure 9
5.2.1. EV9942EF Configuration 9
5.3. Third – Operate 10

6. Signal Lists 11

7. Circuit Schematics and Board Layouts 18

8. Detailed Description 20
8.1. Hardware Description 20
8.1.1. Receiver 20
8.1.2. Local Oscillator (LO) 23
8.1.3. Power Supply 24
8.2. Adjustments and Controls 24
8.2.1. Operation on other Frequency Bands and Configurations 24
8.2.2. Rx I/Q Mixer Input Match (when using J3 input) 24
8.2.3. Internal/External LO 25
8.3. PC Control Software 26
8.3.1. The C-BUS Control Tab 27
8.3.2. The Reg 1 Tab 28
8.3.3. The Reg 2 Tab 29
8.3.4. The Script Handler Tab 30
8.4. Application Information 31
8.4.1. Rx Testing the CMX994EF with the CMX7164 via the PE0601 31
8.5. Troubleshooting 33
8.5.1. General 33
8.5.2. Receiver Operation 34
8.5.3. Transmitter and PLL Operation 35

9. Performance Specification 36
9.1. Electrical Performance 36
9.1.1. Absolute Maximum Ratings 36
9.1.2. Operating Limits 36
9.1.3. Operating Characteristics 37

Table **Page**

Table 1 - Signal List 11
Table 2 - C-BUS Interface 12
Table 3 - Control Interface (Connector J14) 13
Table 4 - Test Loops 15
Table 5 - Test Points 16
Table 6 - Jumper Links 17
Table 7 - Components for Direct Input to I/Q Mixer at 450 MHz 24
Table 8 - Components for Direct Input to I/Q Mixer at 100 MHz 24
Table 9 - Components for Direct Input to I/Q Mixer at 900 MHz 25
Table 10 - Components for use CMX994EF VCO at 440 MHz 25
Table 11 - Possible General Errors 33
Table 12 - Possible Receiver Errors 34
Table 13 - Possible Transmitter Errors 35

Figure **Page**

Figure 1 - Block Diagram 5
Figure 2 - Typical Evaluation Connections for EV9942EF 7
Figure 3 - EV9942EF Connection to PC Using PE0003 8
Figure 4 - USB Driver Installation Message Box 9
Figure 5 - PCB Layout: top 18
Figure 6 - PCB Layout: bottom 19
Figure 7 - LNA S_{21} and S_{12} 450 MHz, 100R mode 21
Figure 8 - Typical LNA S_{11} and S_{22} response 450 MHz, 100R mode 21
Figure 9 - LNA S_{21} and S_{12} 450 MHz, 50R mode 22
Figure 10 - Typical LNA S_{11} and S_{22} response 450 MHz, 50R mode 22
Figure 11 - ACR Filter Response with Different Bandwidth Settings 23
Figure 12 - The C-BUS Control Tab 27
Figure 13 - The Reg 1 Tab 28
Figure 14 - The Reg 2 Tab 29
Figure 15 - The Script Handler Tab 30
Figure 16 - 4QAM, 16QAM and 64QAM Sensitivity Curves 32

2. History

Version	Changes	Date
1.0	First published document as Provisional status	April 2026

Information in this document is subject to change and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues.

It is recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

2.1. Glossary

ACR	Adjacent Channel Rejection
ADC	Analogue to Digital Converter
B/B	Baseband
BER	Bit Error Rate
C-BUS	4-Wire control interface, see CMX994EF datasheet
CW	Continuous Wave
DAC	Digital to Analogue Converter
LNA	Low Noise Amplifier
LO	Local Oscillator
NF	Not Fitted
PC	Personal Computer
PCB	Printed Circuit Board
PER	Packet Error Rate
PLL	Phase Locked Loop
RF	Radio Frequency
Rx	Receiver
TBD	To Be Decided
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Controlled, Temperature Controlled Xtal Oscillator
VGA	Variable Gain Amplifier

ESD Caution

High-performance RF integrated circuits are highly sensitive to electrostatic discharge (ESD) and may contain unprotected inputs and outputs. Handling and assembly should be conducted in an ESD-controlled environment. It is recommended that ESD precautions and protocols are adopted to minimise the risk of electrostatic discharge and protect product integrity.

3. EV9942EF System Block Diagram

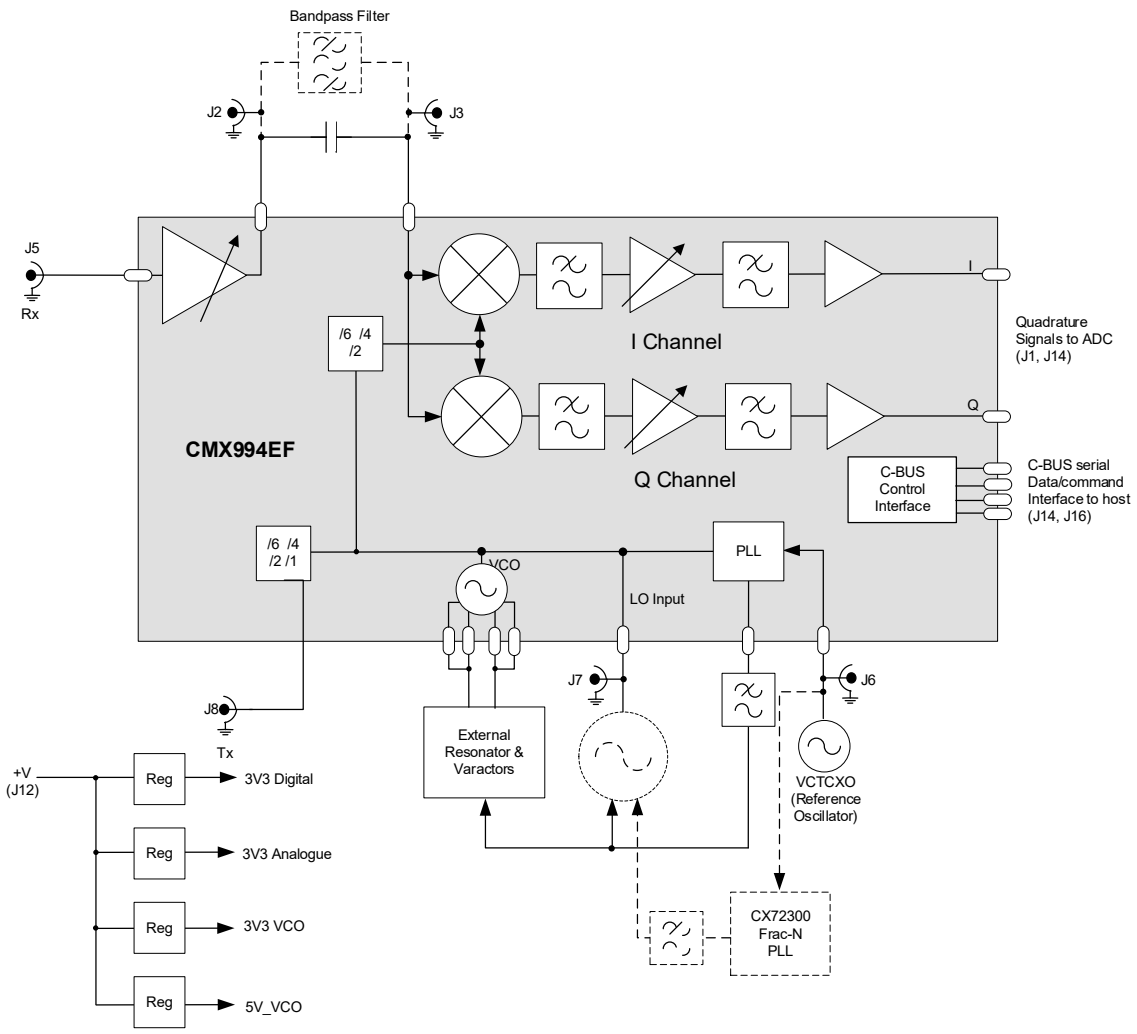


Figure 1 - Block Diagram

4. Preliminary Information

The EV9942EF provides a platform for evaluation of the CMX994EF integrated circuits.

To use the EV9942EF a PC interface or micro-controller is required to control the CMX994EF via its C-BUS interface. This controller is not part of the EV9942EF kit. A separate CML product (PE0003) is available which provides the controller functionality and interfaces to a standard PC by means of a USB cable.

A PC application is available for C-BUS communication, **ES9942EFxx.exe**.

4.1. Laboratory Equipment

The following laboratory equipment is recommended for use with this evaluation kit:

- Power Supply (Dual Power Supply if using PE0003)
- RF Signal Generator(s) (100 MHz to 2 GHz)
- RF Spectrum Analyser (up to 1 GHz)
- Oscilloscope
- Personal Computer + PE0003 or other C-BUS microcontroller

For more detailed design or investigation work, other RF test equipment may be required.

4.2. Power Supply

The supply input voltage to the PCB is 7.2V (5.25 V to 8 V acceptable). On-board regulators are provided to generate all voltage rails used on the PCB (3.3 V and 5 V rails are used). The 7.2 V supply should be rated at 1 A.

NOTE:

1. **Care should be exercised with the power supplies, as they are not protected for reverse polarity.**
2. **When using the EV9942EF kit with a PE0003 kit, power is not supplied to the PE0003 via the C-BUS connector (J16). The PE0003 must be connected to a separate +5V regulated power supply.**

4.3. Handling Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation.

4.3.1. Static Protection

This product uses circuits that can be damaged by electrostatic discharge. Partially damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

4.3.2. Contents - Unpacking

Please ensure that you have received all the items on the separate information sheet (EK9942EF) and notify CML within seven working days if the delivery is incomplete.

4.3.3. Approvals

This evaluation kit is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements which may apply to this product and the radio frequency signals that may emanate from it.

5. Quick Start

This section provides instructions, in three steps, for users who wish to experiment immediately with the evaluation kit at 448 MHz. This is the default frequency of the kit's hardware configuration. A more complete description of the kit and its uses appear later in this document. The EV9942EF includes a CMX994EF integrated circuit**.** Accordingly, before using the EV9942EF, the user should read the current CMX994EF datasheet.

This Quick Start configuration assumes the user has a CML PE0003 Evaluation Kit Interface Card available and that the PE0003 provides the interface between EV9942EF and a controlling PC.

5.1. First – Initial Setup

5.1.1. Make External Connections and Apply Power

Perform the following steps in sequence:

1. Connect test leads as shown below in Figure 2.
2. Connect a controller to C-BUS interface J16 (PE0003 can be used – see Figure 3. Note: J3 or J5 can be used on PE0003, but ensure the correct C-BUS port is selected when programming data: Figure 3 shows PCB connected using port 2).
3. Install PE0003 hardware/software and apply power to PE0003 – see section 5.1.2
4. If not already applied, power should be provided to the main EV9942EF supply (7.2V nominal).

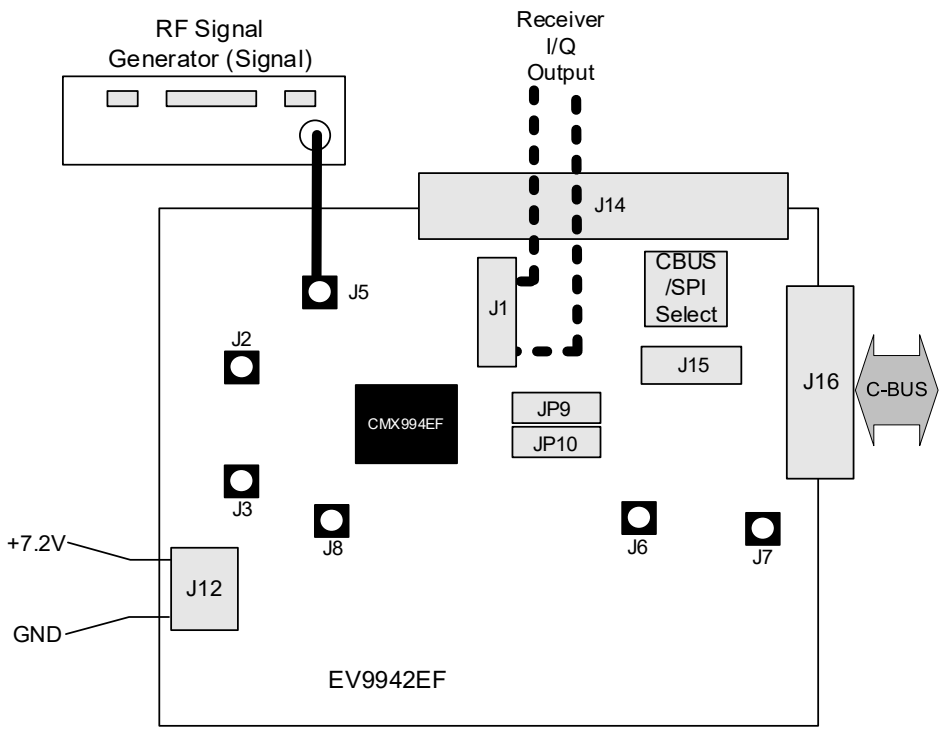


Figure 2 - Typical Evaluation Connections for EV9942EF

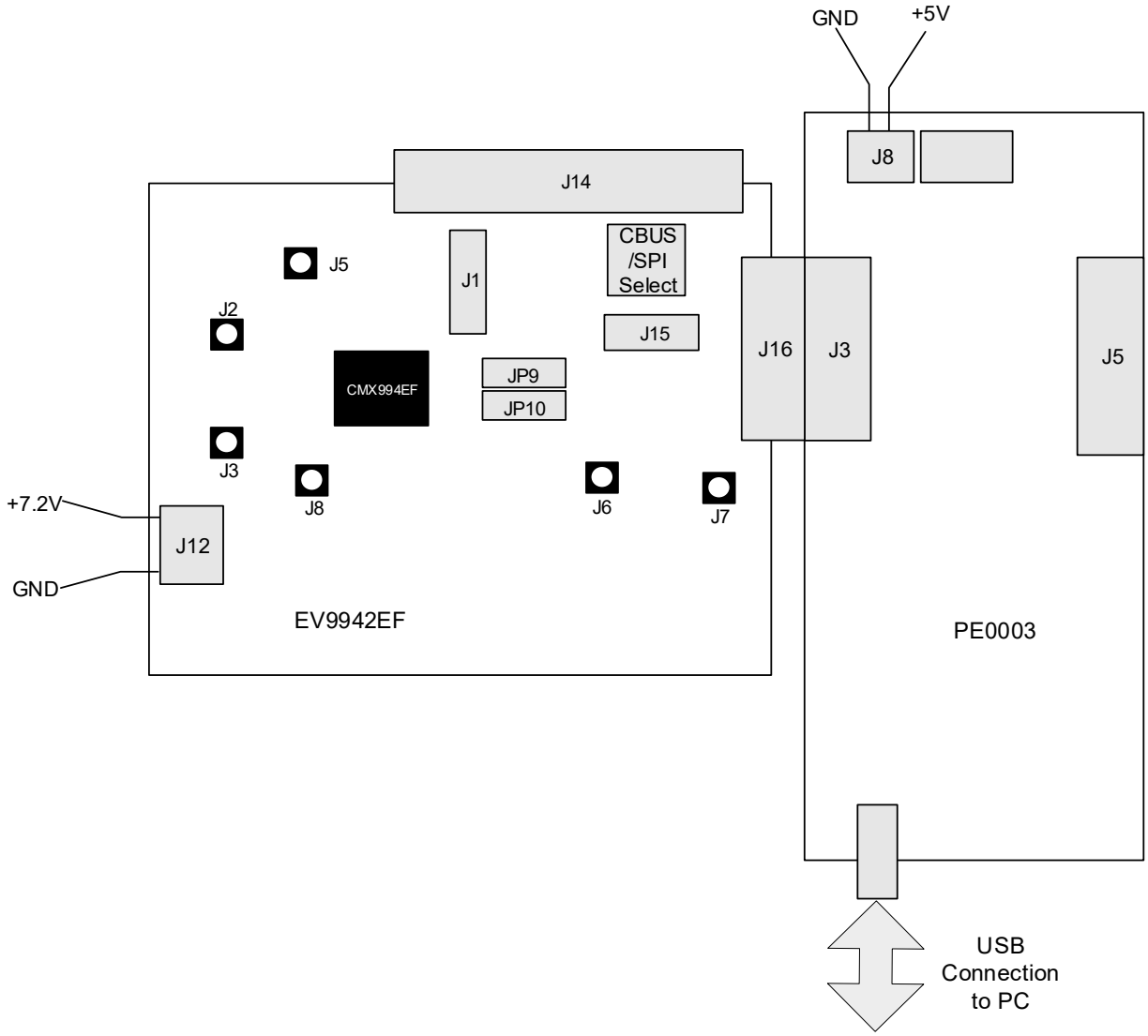


Figure 3 - EV9942EF Connection to PC Using PE0003

5.1.2. Hardware/Software Installation (for PE0003)

- Copy the file '**ES9942EFxx.zip'**, which is downloaded from the CML website following registration, to the hard drive of your host PC.
- Extract the files to the hard drive of your host PC.
- Connect a 5 V dc supply to the PE0003 Interface.
- Connect a 7.2 V dc supply to the EV9942EF.
- Attach a USB cable from connector J2 of the PE0003 Interface Card to the PC USB port.
- Turn on the power supply to the PE0003. The PE0003 power-on indicator D8 will light.
- Install the USB driver when requested. The driver is in the same folder where the '**ES9942EFxx.zip**' files were extracted to, in directory '.\Driver'. Follow instructions on the screen to install the USB driver. Click 'Install this driver software anyway' when the Message Box in Figure 4 is shown.

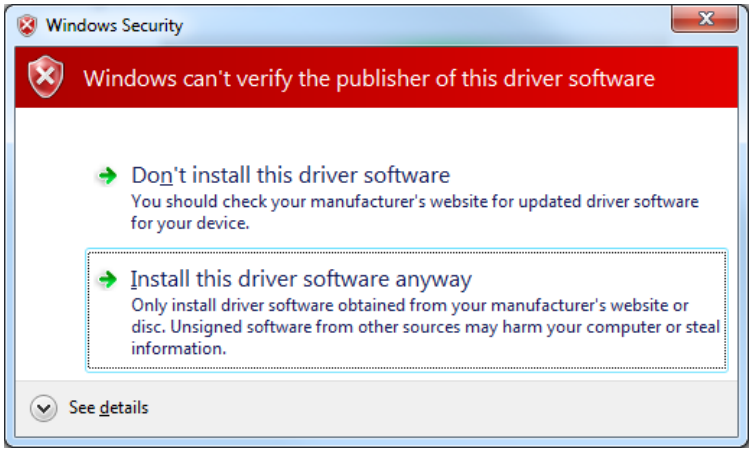


Figure 4 - USB Driver Installation Message Box

5.2. Second – Configure

In this second step the EV9942EF is configured for Rx operation at 448 MHz input frequency.

5.2.1. EV9942EF Configuration

The following steps should be undertaken to configure the EV9942EF to receive at 448 MHz with an I/Q output. Set the applied signals and register values as shown in the following table.

Note: Setting the CMX994EF registers requires the use of the PE0003 host connected as above. The CMX994EF datasheet give details of the registers and commands.

Signal or Register	Setting	Note
LNA_IN (J5)	448.001 MHz	The input level here may be user defined: for example, an input signal of –60 dBm at J5 the typical single-ended output level would be ~440 mVp-p at J1 pin 2. The output should be 1 kHz sine and cosine waves on I and Q when the configuration in this table is completed.
General Reset register ($10)	To ensure the device and hardware are in known states issue the General Reset command	Use RESET script, see section 8.3 for details.
General Control register ($11)	The General Control register should be set to enable the following: • Bias generator • PLL • Rx	Write $86 to register $11. The value $84 may be used if the RXEN pin is used to enable the CMX994EF.
VCO Control register ($25)	Enable the LO input [b4]	Write $10 to register $25.

Signal or Register	Setting	Note
Rx Control register ($12)	Select the LO/2 mode and enable the following: • Rx Mixer and divider • LNA • B/B Differential Amps and filters The filter bandwidth is selected in this register [b4 and b3].	Write $10 to register $12, this enables LO divide by 2 mode, all Rx Circuits on and maximum filter bandwidth.
Rx Offset register ($13) (or Extended Rx Offset ($17))	The value written to this register will vary between devices. A good starting point is $88.	Write $88 to register $13 and then check the dc levels on J1 (I and Q) to ensure the voltage difference between the differential pins of both I and Q channels is less than 20mV; adjust the value written to $13 as required.
Rx Gain register ($16)	Set Rx Gain to maximum.	Write $00 to register $16.
LNA IM Control register ($14)	For optimal IMD performance a value of $3F is recommended.	Write $3F to register $14. The value written to this register can be adjusted to give the optimal IMD performance.
PLL M Divider registers ($20-22) and R divider register ($23-24)	Enable the following: • Charge pump • PLL The default settings for the LO are as follows: • Required frequency = 896 MHz • Comp frequency = 12.5 kHz • Ref frequency = 19.2MHz	The default values would be M = 71680 and R = 1536. Write the following to the relevant register (note that the divider values are updated when register $22 is written so $20 and $21 need to be written first, therefore $23 needs to be written before $24); $22 = $A1, $21 = $18 and $20 = $00 $24 = $06 and $23 = $00 Note: If an external LO is to be used (see 8.2.3) the PLL circuitry (b2 in register $11) and the NR amplifier (b1 in register $25) should be disabled. The LO Input (b4 in register $25) should be enabled.
RXI/Q (J1)	Rx I/Q output.	The differential I and Q signals can be taken from J1.

5.3. Third – Operate

Following the configuration procedures given in sections 5.1 and 5.2, the EV9942EF should be operating as a receiver at 448 MHz. Various evaluation tests can now be performed.

6. Signal Lists

Table 1 - Signal List

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J1	1, 3, 7, 9	NC	Baseband	Not connected
J1	2	RXI+	Baseband	I channel positive output
J1	4	RXI-	Baseband	I channel negative output
J1	5, 6	GNDA	DC	Ground (analogue)
J1	8	RXQ-	Baseband	Q channel negative output
J1	10	RXQ+	Baseband	Q channel positive output
J2	N/A	LNA_OUT	RF	Test connector to observe LNA output. To use this connector C7 must be fitted; C1 and C15 not fitted.
J3	N/A	Rx_MIXIN	RF	Test connector to allow direct input to the I/Q down-converter mixers (no LNA). To use this connector C8 must be fitted; C2 and C15 not fitted.
J5	N/A	LNA_IN	RF	LNA input
J6	N/A	REFIN	RF	Input for external reference source for PLL. To use this input C34 needs to be fitted to the PCB and C31, R16 removed.
J7	N/A	LO	RF	Main LO input or external VCO output
J8	N/A	TXLO_OUT	RF	Tx LO Output
J12	2	+V	DC	7.2V power supply input
J12	1	GND	DC	Power supply ground
J14	1 – 62			See Table 3
J15	1, 5	GNDD	DC	Ground (digital)
J15	2	RF_MOSI	Logic	Data input for PLL programming interface
J15	3	RF_SCLK	Logic	Clock for PLL programming interface
J15	4	RF_CSN	Logic	Latch/Enable for PLL programming interface
J16	1 – 20	C-BUS Interface	Logic	C-BUS interface from PE0003 or host controller. See schematics, CMX994EF Datasheet and Table 2 for details.

Table 2 - C-BUS Interface

CONNECTOR PINOUT for J16			
Connector Pin No.	**Signal Name**	**Signal Type**	**Description**
1	RESETN	I/P	General RESET (RESET active low)
2	CSN	I/P	C-BUS Enable.
3	-	-	Spare pin. Leave unconnected.
4	CDATA	I/P	C-BUS Data Input.
5	-	-	Spare pin. Leave unconnected.
6	SCLK	I/P	C-BUS Clock.
7	-	-	Spare pin. Leave unconnected.
8	RDATA	O/P	C-BUS Data Output.
9	-	-	Spare pin. Leave unconnected.
10	IRQN	I/P	Interrupt request - if required. Not used, so remains unconnected on EV9942EF.
11	GNDD	Power	Connection to Digital Ground.
12	GNDD	Power	Connection to Digital Ground.
13	-	-	Spare pin. Leave unconnected.
14	-	-	Spare pin. Leave unconnected.
15	-	-	Spare pin. Leave unconnected.
16	-	-	Spare pin. Leave unconnected.
17	-	-	Spare pin. Leave unconnected.
18	-	-	Spare pin. Leave unconnected.
19	-	-	Spare pin. Leave unconnected.
20	-	-	Spare pin. Leave unconnected.

Notes: I/P = Input
O/P = Output

Table 3 - Control Interface (Connector J14)

CONNECTOR PINOUT for J14			
Connector Pin No.	**Signal Name**	**Signal Type**	**Description**
1	RF_MOSI	I/P	Data input for PLL programming interface
2	RF_SCLK	I/P	Clock for PLL programming interface
3	MOSI	I/P	SPI Command Data (Master Out Slave In)
4	MISO	O/P	SPI Read Data (Master In Slave Out)
5	GNDD	GND	Digital ground
6	GPIO13	I/P	Not connected
7	SSOUT	I/P	SPI Chip Select
8	GNDD	GND	Digital ground
9	GPIO11	I/P	Not connected
10	GNDD	GND	Digital ground
11	NC	-	Not used on EV9942EF – do not connect to this pin
12	+V_EXT	I/P	+5V (nominal) power (not used on EV9942EF)
13	+V_EXT	I/P	+5V (nominal) power (not used on EV9942EF)
14	GNDA	GND	Analogue ground
15	19M2_TCXO	BI	19.2 MHz VCTCXO input (To use, fit C36 and R79. Do not fit C31&R16)
16	AUXDAC0	I/P	Not connected
17	AUXDAC2	I/P	Not connected
18	GNDA	GND	Analogue ground
19	AUXADC3	O/P	Not connected
20	AUXADC1	O/P	Not connected
21	GNDA	GND	Analogue ground
22	IP1	O/P	Not connected
23	IP2	O/P	Not connected
24	SPKR_2_OP	O/P	Not connected
25	MOD1P	I/P	Not connected
26	MOD1N	I/P	Not connected
27	EXT_VBIAS	I/P	Not connected
28	NC	-	Not connected
29	MOD2P	I/P	Not connected
30	MOD2N	I/P	Not connected
31	GNDA	GND	Analogue ground
32	J14_RXI+	O/P	Rx I channel positive output

CONNECTOR PINOUT for J14 (cont'd)			
Connector Pin No.	**Signal Name**	**Signal Type**	**Description**
33	J14_RXI-	O/P	Rx I channel negative output
34	GNDA	GND	Analogue ground
35	GNDA	GND	Analogue ground
36	GNDA	GND	Analogue ground
37	GNDA	GND	Analogue ground
38	J14_RXQ+	O/P	Rx Q channel positive output
39	J14_RXQ-	O/P	Rx Q channel negative output
40	GNDA	GND	Analogue ground
41	AUXADC0	O/P	Not connected
42	AUXADC2	O/P	Not connected
43	GNDA	GND	Analogue ground
44	AUXDAC3	I/P	Not connected
45	AFC	I/P	AFC input (AUXDAC1)
46	GNDA	GND	Analogue ground
47	GNDA	GND	Analogue ground
48	GNDA	GND	Analogue ground
49	+V_EXT	I/P	+5V (nominal) power (not used on EV9942EF)
50	NC	-	Not used on EV9942EF – do not connect to this pin
51	GNDD	GND	Digital ground
52	GPIO10	I/P	Not used on EV9942EF – do not connect to this pin
53	GNDD	GND	Digital ground
54	RX_EN	I/P	GPIO4 – Rx Enable on the EV9942EF
55	TX_EN	I/P	GPIO0 – Rx Enable on the EV9942EF
56	GNDD	GND	Digital ground
57	GPIO5	I/P	Not connected
58	CLK/CLK0	I/P	SPI Clock
59	RF_CSN	I/P	Latch/Enable for PLL programming interface
60	GPIO1	-	Not connected
61	NC	-	Not connected
62	NC	-	Not connected

Table 4 - Test Loops

TEST LOOPS		
Test Loop Ref.	**Default Measurement**	**Description**
TL5	-	C-BUS Serial Data Input
TL8	0V	Analogue ground
TL9	0V	Digital ground
TL14	-	Optional serial 'Mod_in' data for the EXT PLL

Notes:

I/P	=	Input
O/P	=	Output
BI	=	Bidirectional
TL	=	Test Loop
TP	=	Test Point

Table 5 - Test Points

TEST POINTS		
Test Point Ref.	**Default Measurement**	**Description**
TP1	3.3V	VDDIO
TP3	-	AFC (Automatic Frequency Control) to VCTCXO, U2
TP4	0V	Analogue ground
TP5	-	PLL Loop filter output/VCO control voltage
TP7	3.3V	3.3V regulator output for digital circuits
TP8	3.3V	3.3V regulator output for analogue circuits
TP9	3.3V	3.3V regulator output for VCO/PLL circuits
TP10	5.0V	5.0V regulator output for VCO/PLL circuits
TP11	-	IRQN (C-BUS IRQN, not used on EV9942EF)
TP13	-	EXT PLL (U8) PLL Loop filter output
TP14	-	EXT PLL (U8) Lock Detect output pin
TP15	-	EXT PLL (U8) ‘Mux_Out’ pin
TP16	-	IFLT1N Receiver post mixer monitoring point (I channel)
TP17	-	IFLT1P Receiver post mixer monitoring point (I channel)
TP18	-	QFLT1N Receiver post mixer monitoring point (Q channel)
TP19	-	QFLT1P Receiver post mixer monitoring point (Q channel)

Table 6 - Jumper Links

JUMPERS/LINKS			
Link Ref.	**Positions**	**Default Position**	**Description**
JP1	1-2	1-2	Connects on-board regulator (1-2) or allows an external power supply to be connected (NF), +3V3D
JP2	1-2	1-2	Connects on-board regulator (1-2) or allows an external power supply to be connected (NF), +3V3A
JP3	1-2	1-2	Connects on-board regulator (1-2) or allows an external power supply to be connected (NF), +3V3_VCO
JP4	1-2	NF	Connects on-board regulator (1-2) or allows an external power supply to be connected (NF), +5V_VCO
JP5	1-2	NF	Selects SPI MISO from Host (1-2), if required
JP6	1-2/2-3	NF	Selects between SPI CSN (1-2) or PLL programming CSN (2-3)
JP7	1-2/2-3	NF	Selects between SPI CLK (1-2) or PLL programming CLK (2-3)
JP8	1-2/2-3	NF	Selects between SPI MOSI (1-2) or PLL programming MOSI (2-3)
JP9	1-2/2-3	2-3	Rx Enable, can select between +3V3D (1-2) and GNDD (2-3)
JP10	1-2/2-3	2-3	Tx Enable, can select between +3V3D (1-2) and GNDD (2-3)

7. Circuit Schematics and Board Layouts

Circuit schematics are available as high-resolution files. These can be obtained via the CML website, file: '**Dwg9942EFA02.pdf**'.

The layout on each side of the PCB is shown in Figure 5 and Figure 6.

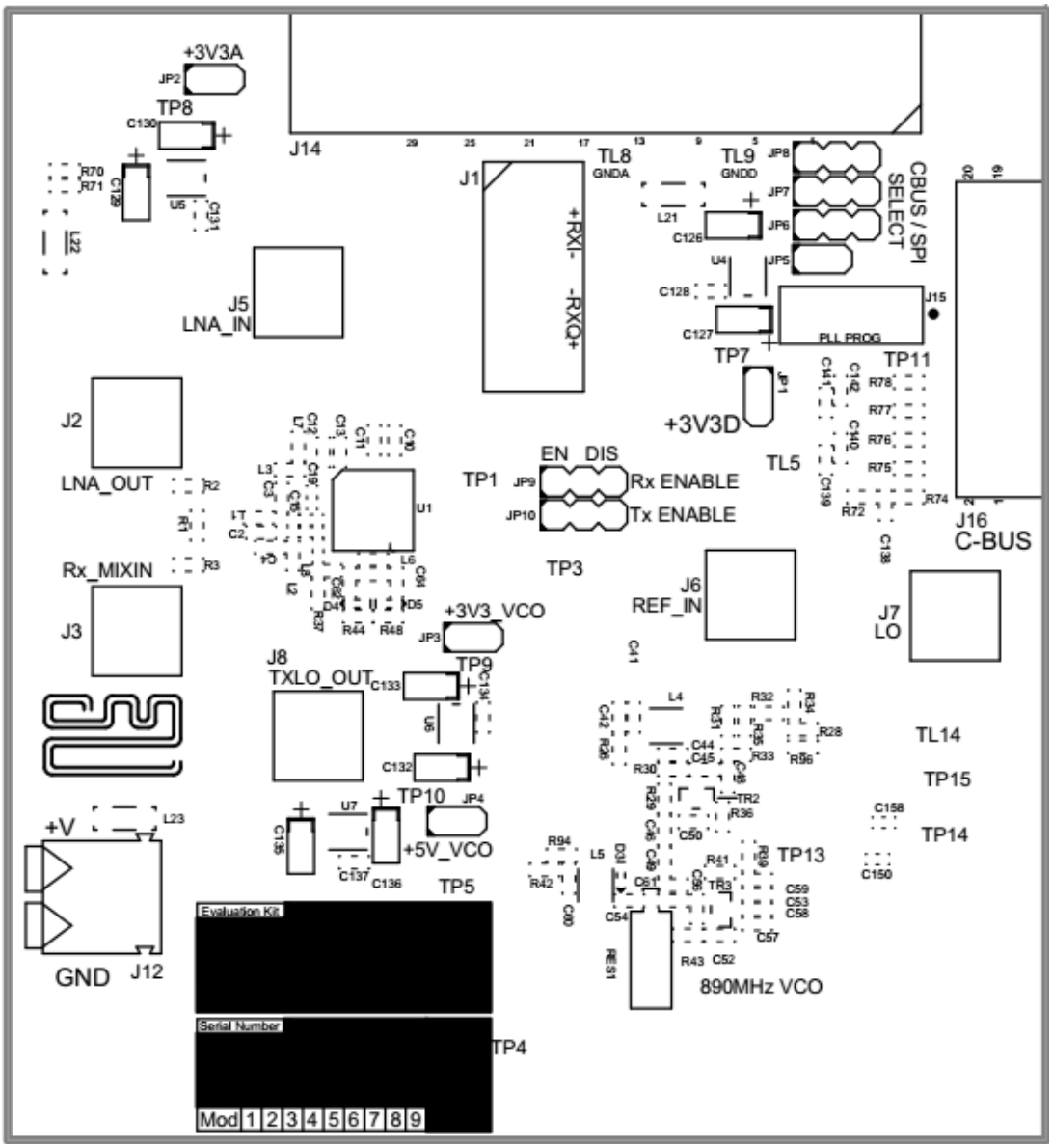


Figure 5 - PCB Layout: top

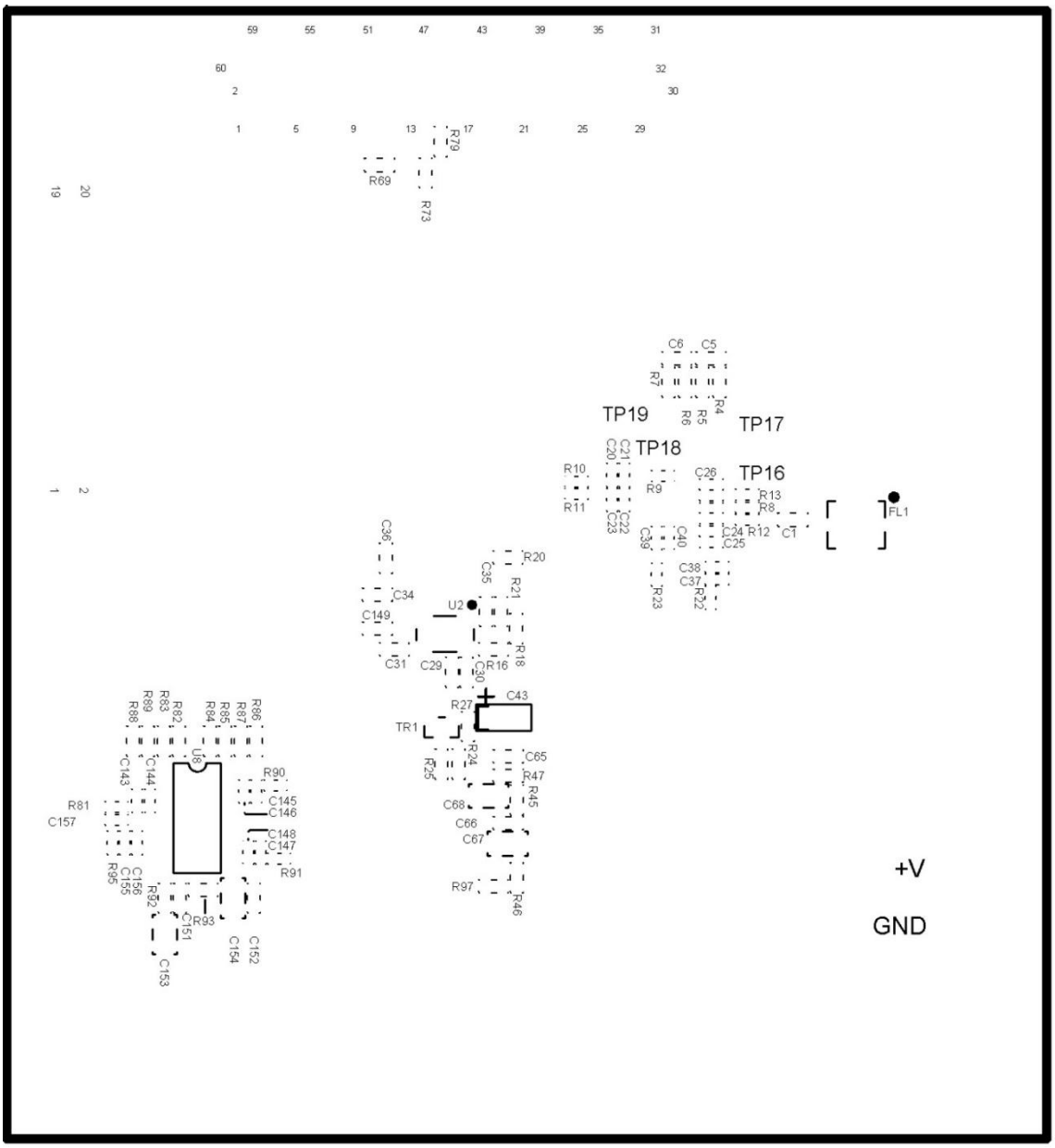


Figure 6 - PCB Layout: bottom

8. Detailed Description

Refer to the CMX994EF datasheet for a detailed description of the device.

The EV9942EF functionality includes:

- Demonstration of a linear direct conversion receiver from RF input to output in I/Q format including:
  - LNA with gain control
  - I/Q mixers
  - first baseband filters
  - first baseband amplifiers
  - second baseband filters
  - second baseband amplifiers
- VCO, Integer-N PLL and divider.
- Tx LO Output.
- Operation 100 MHz to 1000 MHz (448 MHz = default configuration).
- 19.2 MHz VCTCXO.
- On-board linear regulators for all necessary power rails.
- The C-BUS Interface that allows the card to be connected to a host µController. A PC Interface board is separately available and allows control of all device functions, to support initial test and customer evaluation.
- Interface to CMX7164/CMX7364 evaluation boards (PE0601-7164 / PE0602-7364, not included) to allow demonstration/test of QAM and 2-FSK / 4-FSK demodulation.
- Interface to CMX7341 evaluation card (PE0403, not included) to allow demonstration/test with FSK demodulation including functionality for dPMR, Analogue PMR, NXDN, APCO P25 radio standards.
- Interface to CMX983 evaluation card (EV9830, not included) allows demonstration of:
  - Linear receiver
  - Pi/4-DQPSK

In summary, the EV9942EF allows the user to create experiments to investigate all aspects of the CMX994EF device. The EV9942EF is designed to allow user modification, to support the detailed investigation of the user's specific and different applications. The evaluation platform also includes additional circuits that may be used to evaluate system performance, for example a high-frequency VCO (TR2/TR3).

8.1. Hardware Description

8.1.1. Receiver

The EV9942EF demonstrates the CMX994EF advanced direct conversion receiver IC, which is capable of supporting a range of digital radio systems of both constant envelope and linear modulation types. The applied input signal, typically applied at J5, will be amplified by the on-chip LNA. The output of the LNA may be either matched to the input of the I/Q down-conversion mixers by C7, L1, C15 and C8, or passed through an external filter FL1. Alternatively, the signal may be passed to test connector J2 for detailed LNA test and measurement purposes.

The I/Q down-conversion mixers can be accessed from test connector J3 or driven from the LNA, as previously described. The mixers convert the received signal to I/Q baseband format, where C10 and C12 combine with on-chip components to remove off-channel signals. The signal is then amplified before further filtering is provided to remove adjacent channel signals. A final amplifier stage completes the receiver line-up, providing differential I/Q outputs.

Typical performance of the CMX994EF; overall receiver gain and noise figure for the default configuration is ~63 dB and 4 dB respectively. The Rx IIP3 (input third-order intercept point) achieved is ~ -2 dBm.

8.1.1.1. LNA

The CMX994EF includes a broadband LNA. The design has a single-ended input and output. This minimises cost and board area, as balun transformers are not required. The LNA can be evaluated using J5 (input) to J2 (output). The plots in Figure 7 to Figure 10 show typical performance of the LNA with the input and output matched to 450 MHz.

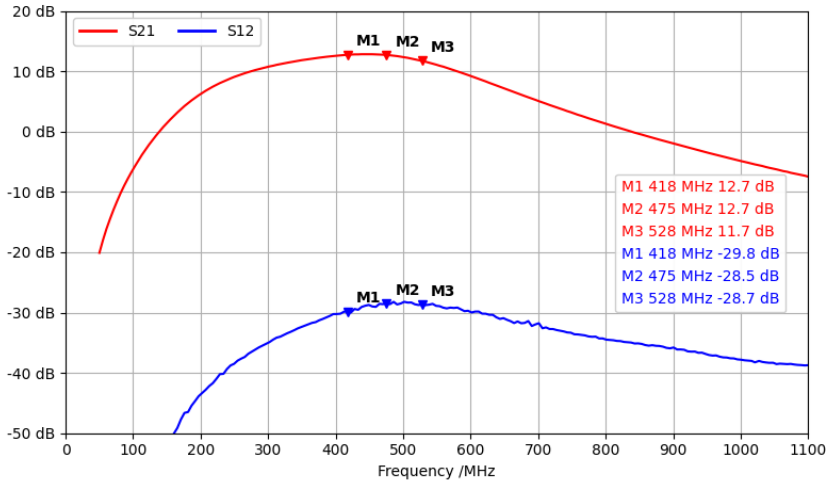


Figure 7 - LNA S_{21} and S_{12} 450 MHz, 100R mode

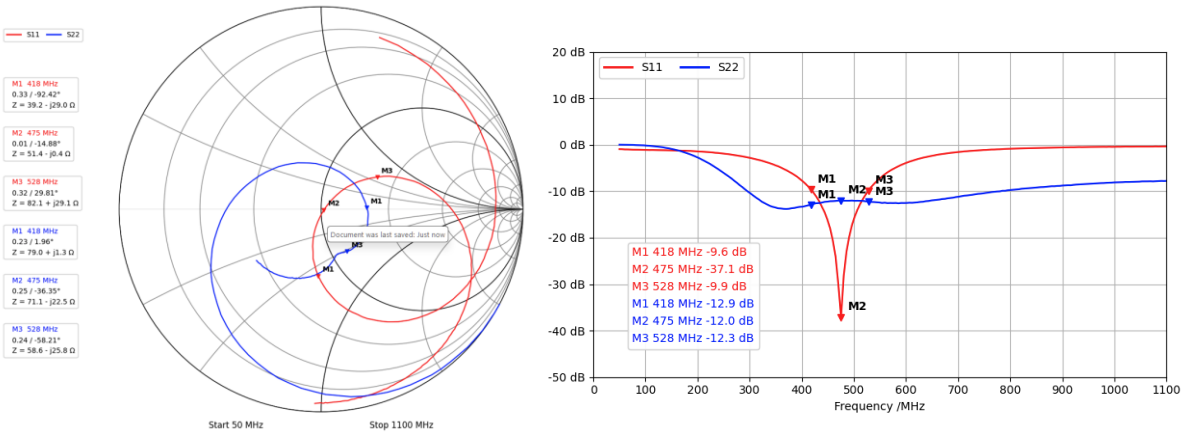


Figure 8 - Typical LNA S_{11} and S_{22} response 450 MHz, 100R mode

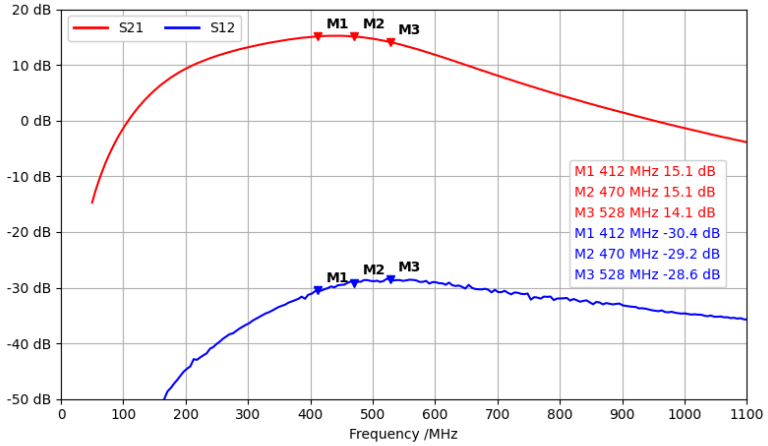


Figure 9 - LNA S_{21} and S_{12} 450 MHz, 50R mode

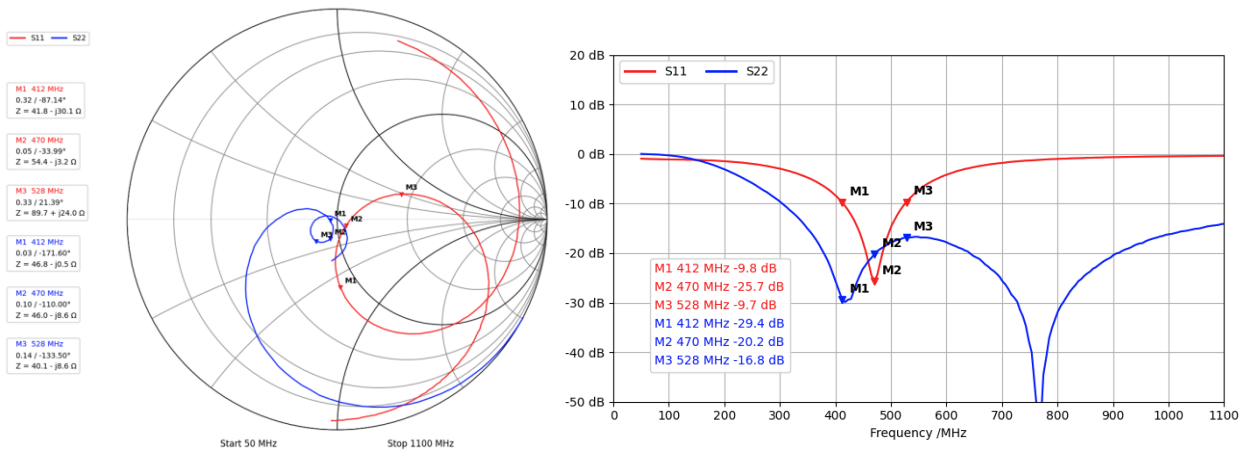


Figure 10 - Typical LNA S_{11} and S_{22} response 450 MHz, 50R mode

8.1.1.2. Rx Direct Conversion Mixers and Filtering

The Rx I/Q Mixers have a single-ended input with a nominal input frequency range of 100 MHz to 1000 MHz for the CMX994EF. When the mixer is connected to the LNA, a simple interstage match is required. See the CMX994EF datasheet for further details of the interstage match component values for different operating frequencies; the default build of the EV9942EF is for operation 450 MHz. The mixer has selectable LO input dividers: these are /2, /4 and /6.

The output of the I/Q mixers is baseband; the two capacitors (C10, C12) together with on-chip components determine the break point of a first stage of baseband filtering, intended to attenuate off-channel signals such as blockers and signals used in intermodulation testing.

After the filters, a variable gain amplifier is provided, followed by a further stage of filtering. Again, external capacitors (C11, C13) set the response of the filter. Resistor R9 is provided to act as a reference to ensure the accuracy of the filter response. For details of the filter configurations and how to adjust the values see the CMX994EF datasheet. The filter bandwidth can be scaled on a ratio of 1:2:4, typical results are shown in Figure 11, again see the CMX994EF datasheet for further details.

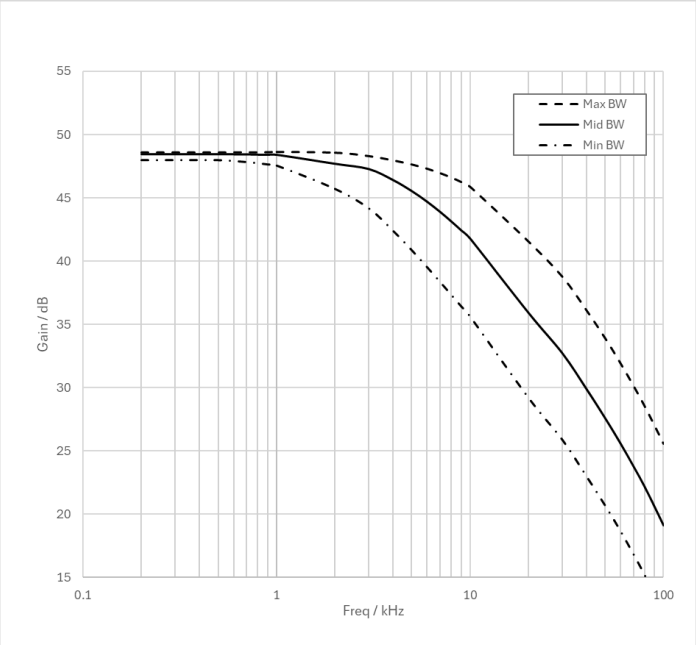


Figure 11 - ACR Filter Response with Different Bandwidth Settings

The I/Q chain is completed by a final stage of amplification, which drives the differential output pins on the CMX994EF IC (RXIP, RXIN, RXQP, RXQN). These outputs are available on the EV9942EF board as RXI+, RXI-, RXQ+ and RXQ-.

8.1.1.3. DC Offset Correction

The EV9942EF does not provide direct compensation of DC offsets in the I/Q outputs from the receiver, however the CMX994EF does allow a coarse DC offset compensation to be applied to maximise receiver dynamic range; this assumes that the I/Q signals are measured externally to calculate the required compensation. See the CMX994EF datasheet for further details.

8.1.2. Local Oscillator (LO)

8.1.2.1. CMX994EF VCO and PLL

The EV9942EF provides components to use the VCO amplifier and PLL contained within the CMX994EF IC. As supplied, the resonator circuit (L6, C63, C62, C64, D4, D5) is configured for 440 MHz operation with a tuning sensitivity of approximately 20 MHz/V. The component values used for the PLL loop filter provide a bandwidth of approximately 1 kHz. The oscillator is usable up to about 1 GHz, for further details consult the CMX994EF datasheet, see also section 8.2.3.

8.1.2.2. EV9942EF Alternative VCO

The EV9942EF PCB includes an external VCO (TR2/TR3) for improved phase noise operation. The external VCO uses a ceramic resonator (RES1) and is thus flexible in its operation. The default components give an operating frequency at around 896 MHz, allowing operation of the IC at 448 MHz when the Rx divider is in /2 mode. This VCO is connected to the CMX994EF LO input (LOP, pin 12). To allow testing at frequencies not directly supported by the VCOs on the PCB, an external LO signal may be applied to J7. If an external LO is used it is recommended that the on-chip and on-board VCOs are disabled (e.g. by ensuring R24 and R25 are not fitted).

8.1.2.3. EV9942EF Alternative PLL

Some CMX994EF applications may require a Fractional-N PLL, it is recommended to consider the CMX940 Low Power High Performance RF Synth with Integrated VCO for applications that demand this functionality and the CMX940 can be used in high performance applications (use the following link for further information - CMX940 – Low Power High Performance RF Synth with Integrated VCO | CMLMicro)

8.1.2.4. Reference Oscillator

A 19.2 MHz VCTCXO is fitted on the EV9942EF. An external reference oscillator applied to J6 may be used by fitting C34 with 1 nF and removing C31 and R16. Alternatively, an external oscillator may be connected using J14, in which case C36 should be fitted as 1 nF and C34, C31 and R16 should all be unfitted (NF).

8.1.3. Power Supply

The input to the PCB is nominally 7.2 V (5.25 V to 8 V is acceptable). On board regulators are provided to generate voltage rails used on the EV9942EF.

8.2. Adjustments and Controls

The user has the facility to configure the EV9942EF for a number of different operational scenarios.

8.2.1. Operation on other Frequency Bands and Configurations

The default operating frequency for the as-built EV9942EF is 448 MHz. An application note describing alternative operating bands that are commonly used is available on the CML Micro website on the CMX994EF product page in the design resources section. It also provides guidance on what spurious responses that should be considered within a direct conversion architecture.

8.2.2. Rx I/Q Mixer Input Match (when using J3 input)

For test purposes it may be useful to connect directly to the I/Q down-conversion mixers. This can be done by using J3, the default values for C4 and L2 are for operation at 450 MHz as a complete chain. To use J3 it is necessary to remove C15. The values shown in Table 7 are for operation at 450 MHz. These values provide a match to 50 Ω. In Table 8 and Table 9 are some typical input matching values for 100 MHz and 900 MHz operation respectively. For other operating frequencies refer to the CMX994EF datasheet for details of the mixer input impedance, a s1p file of the mixer input unmatched is available on the CML Micro website for matching networks to be developed.

Table 7 - Components for Direct Input to I/Q Mixer at 450 MHz

Ref. Designator	Values for 450 MHz
C4	4. 7 pF
L2	27 nH
C8	1 nF

Table 8 - Components for Direct Input to I/Q Mixer at 100 MHz

Ref. Designator	Values for 100 MHz
C4	22 pF
L2	150 nH
C2	1 nF

Table 9 - Components for Direct Input to I/Q Mixer at 900 MHz

Ref. Designator	Values for 900 MHz
C4	3.3 pF
L2	6.8 nH
C2	100 pF

8.2.3. Internal/External LO

The EV9942EF has four options for the Local Oscillator. The default configuration of the EV9942EF is to use the external VCO (TR3/TR2) along with the CMX994EF internal PLL. The second option is to use the CMX994EF internal VCO, this can be used for VHF applications in its default configuration. The third option for the EV9942EF is to apply an external LO using J7. The final option is to use the external LO input J7 to inject a LO signal from an external signal generator or from an EV9400 evaluation kit if the system performance is to be evaluated with the CML CMX940 High Performance fractional N PLL with integrated VCO.

To use the CMX994EF internal VCO the following modifications (Table 10) are required. With this configuration the VCO should operate at circa 440 MHz.

Table 10 - Components for use CMX994EF VCO at 440 MHz

Ref. Designator	Values to use CMX994EF VCO
D3 and D4	SMV1705-079LF
L6	8.2 nH[1] (as fitted)
C63	8.2 pF (as fitted)
C62 and C64	22 pF (as fitted)
R46	0 R
R42	NF
C65	150 nF
C66	15 nF
C68	1000 nF
R45	2.4 kΩ
R47	1.5 kΩ

To use the external LO connector (J7), R24 and R25 should not be fitted (NF), to disable the on-board external VCO. The CMX994EF VCO buffer and negative resistance amplifier should be disabled using the General Control Register or the VCO Control Register.

To use the internal VCO the external VCO should be disabled (R24 and R25 should not be fitted) and VCO Negative Resistance amplifier and VCO buffer enabled (e.g. VCO Control Register ($25) set to 0x03, see CMX994EF datasheet for details).

The LO input should be enabled when using an external source (e.g. VCO Control Register ($25) set to 0x10, see CMX994EF datasheet for details).

[1] The quality factor of inductor used must be >50 this is important to ensure that the best performance from the VCO is obtained.

8.3. PC Control Software

The EV9942EF itself does not require any embedded firmware, however, it does require C-BUS control from an external microcontroller. The CML product, PE0003, can be used with the EV9942EF and PC software files '**ES9942EFxx.zip**'. To use the software, connect the EV9942EF as shown in Figure 3. First ensure the drivers supplied for the PE0003 are installed correctly. The executable must be in the same folder on the PC as the '**EF0003xx.bin**' file. Run the '**ES9942EFxx.exe**' and the main application window will open with a progress bar for the initialisation process.

To perform a General Reset on the CMX994EF, a single write to register $10 is required. The following script, which may be used with the **ES9942EFxx** software, is recommended.

```
;General Reset.pes
;This script will send a C-BUS General reset.
;Reset C-BUS (assigns register RESET a zero length parameter to get a single 8-bit write)
;format: register <device (1 or 2)> <C-BUS address> <# parameter bytes (0 to 2)>

RESET const $10
        register 1 RESET 0
        copy 0 *RESET

;If using C-BUS port 2 then use the following lines
;       register 2 RESET 0
;       device 2
;       copy 0 *RESET
```

There are three tabs that represent a particular set of registers or a particular function of the CMX994EF. To select a tab simply click on the corresponding name in the row at the top of the program window. Setting or clearing the check box associated with a bit of a register will cause that bit to be set or cleared when the register is next written to. If the 'Auto Write' check box is set a register will be written whenever a check box or list box associated with it is modified. This removes the need to click the 'Write' button associated with that register. The program can be closed at any time by clicking the 'Close' button or by pressing 'Alt' and 'F4' keys simultaneously.

Note: The C-BUS Control tab and Script Handler tab displays are the same for all three devices. Therefore, a single screen shot has been included for these tabs. Separate screen shots are shown for the Reg 1 and Reg 2 tabs, to show the differences.

8.3.1. The C-BUS Control Tab

The C-BUS Tab allows the user to read from or write to any register plus issue a General Reset command, see Figure 12. Also on this tab, the Hardware Reset command can be issued and the C-BUS header to be used can be selected.

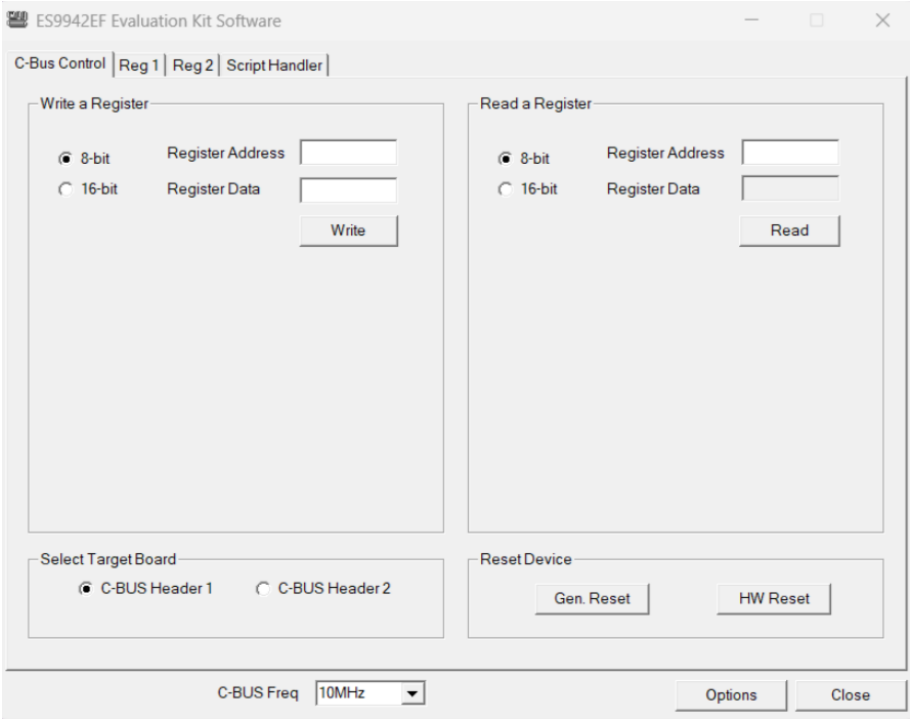


Figure 12 - The C-BUS Control Tab

8.3.2. The Reg 1 Tab

The Reg 1 tab gives the user access to the General Control register, Rx Control register, Rx Offset register, Intermodulation Control register, the Rx Gain register, the Extended Offset register and the Options Control register, see Figure 13. All registers can be written to individually, or as a whole mass register write (Write All bottom left-hand bottom corner of window). If Auto Write is checked, the register is changed as the user makes changes to the register window.

In the case of the Rx Offset and Intermodulation registers, slide bars have been used to allow easy control during operation.

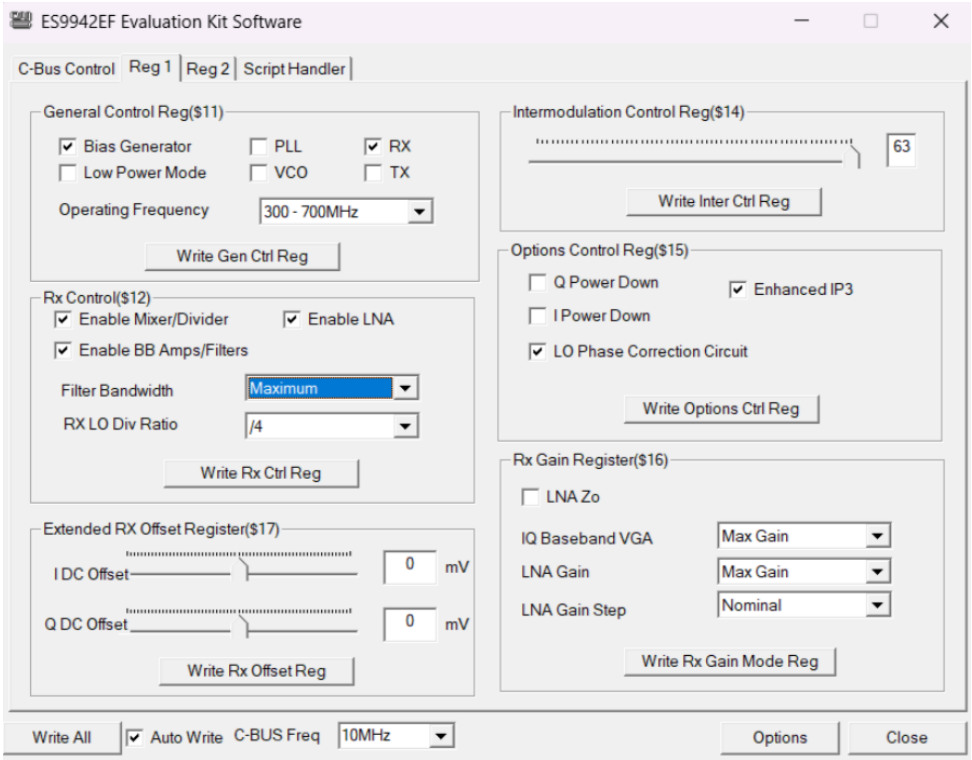


Figure 13 - The Reg 1 Tab

8.3.3. The Reg 2 Tab

The Reg 2 tab gives the user access to the PLL M/R Divider registers and the VCO Control register. All register states can be read with one button press, see Figure 14. All registers can be written to individually, or as a whole mass register write (Write All bottom left-hand bottom corner of window). If Auto Write is checked, the register is changed as the user makes changes to the register.

The PLL M/R Divider register window has a box which indicates the PLL lock detect states. The lock detect is read each time the PLL divider values are written and the status updated. The box will be blank to indicate PLL is out of lock and when the PLL is in lock the box will have an L in it, as shown in Figure 14.

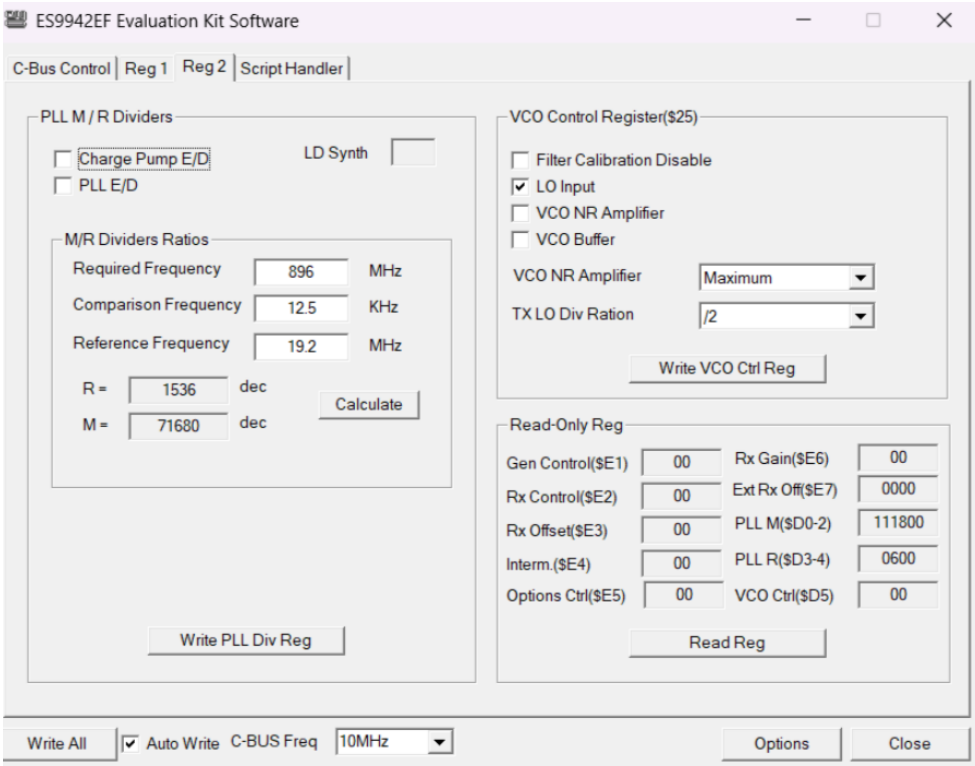


Figure 14 - The Reg 2 Tab

8.3.4. The Script Handler Tab

The Script Handler Tab (shown in Figure 15) allows the execution of script files consisting of register write, read, and delay commands. These are plain text files on the PC, which are compiled via the GUI but executed by the LPC4330 microprocessor on the PE0003 board. The script language is documented separately in the "Script Language Reference" document, which can be downloaded with the PE0003 support package from the CML website. Control of the EV9942EF does not require the use of script files.

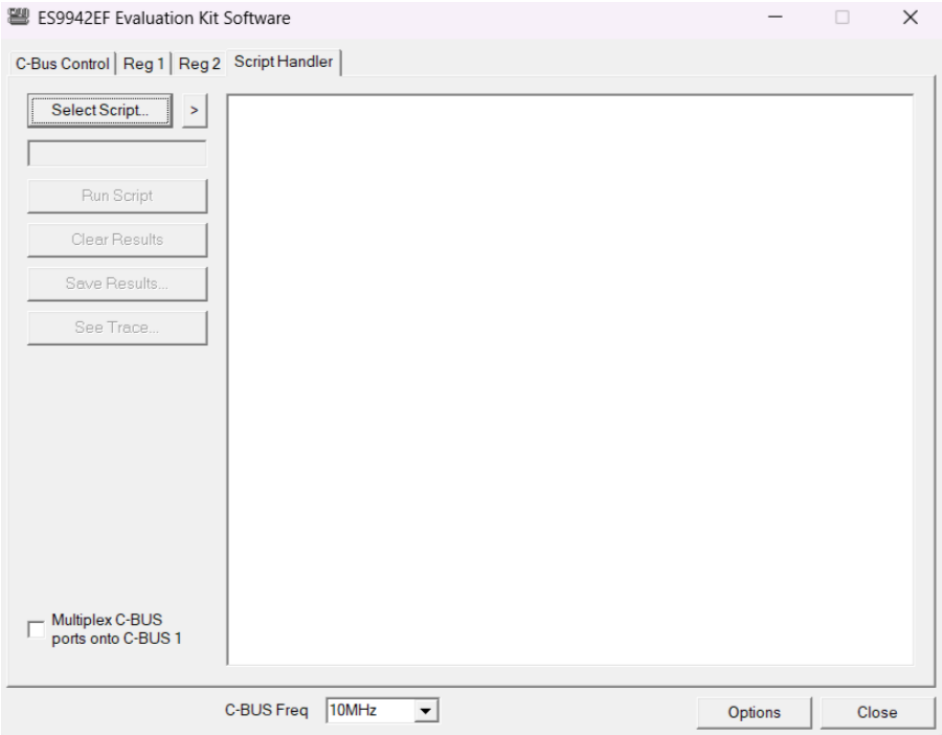


Figure 15 - The Script Handler Tab

To select a script file, click on the 'Select Script' button. The Open File Dialog is displayed. Browse and select the script file. The folder that contains the script file will be the working folder of the script (i.e. all the files referenced in the script will be searched in this folder). Alternatively, select a script file from the recent files list. Click on the '>' button to display the list.

The results window displays the values returned by the script. These results can be saved to a text file or discarded by clicking on the 'Save Results' or 'Clear Results' buttons, respectively. When a script file is being executed the 'Run Script' button will change to the 'Abort' button, the rest of the tab will be disabled and the other tabs cannot be selected.

After a script has finished running and when trace data is available, the 'See Trace…' button will be enabled. Up to 131072 C-BUS transactions can be logged in the PE0003 board. Click in the 'See Trace…' button to display the Trace dialog box. Note that the C-BUS transactions are only logged if the feature has been enabled in the script. See the "Script Language Reference" document for details.

8.4. Application Information

8.4.1. Rx Testing the CMX994EF with the CMX7164 via the PE0601

The EV9942EF has an I/Q interface which may be connected to a PE0601 through J14. This connector also allows the CMX994EF to be programmed via the SPI of the CMX7164. This allows evaluation of the CMX994EF receiver with 4-FSK and QAM modulation (4, 16 and 64QAM). The following results have been taken based on measurement methods and limits taken from EN 301 166 (6.25 kHz channels), EN 300 113 (25 kHz channels, 4-FSK) and EN 302 561 (QAM).

8.4.1.1. Results with 4-FSK

- *Typical Performance 4-FSK, 3 kHz Deviation, 19 200 bps*
  The following performance is considered typical of CMX994EF operation in a 25 kHz RF channel. All results stated are at BER < 1e-2 and in most cases the wanted signal level is -110 dBm for the interferer tests.

  - Sensitivity ~ -116 dBm
  - Intermodulation ~ 65.5 dB
  - Blocking ~ 86 to 93 dB
  - Adjacent Channel Rejection ~ 66 dB (on-board VCO)
  - Adjacent Channel Rejection ~ 72 dB (external LO source)
  - Spurious Response Rejection ~ 75 dB

  The Intermodulation rejection is typically better than 65 dB for <1% BER, with a wanted signal at -107 dBm and interfering signals spaced at 50/100 kHz (tested as EN 300 113).

  Blocking results were taken with an unmodulated interferer at +/-1 MHz offset. Typical blocking measurements are between 86 dB and 93 dB, depending on offset and measurement method (TIA or ETSI).

  The above shows the on-board VCO is limiting the ACR measurement and the measurements with an external LO, for example the CMX940, show that the receiver is capable of achieving >70 dB adjacent channel performance. The CMX994EF maximum filter bandwidth was used when taking all these results. The positive and negative offsets have very similar performance.

  Spurious response test results were measured with a FM modulated interferer at +50 kHz.

8.4.1.2. Typical Performance 4-FSK, 1.05 kHz Deviation, 4800 bps

The following performance is considered typical of CMX994EF operation in a 6.25 kHz RF channel. These measurements were taken with the on-board VCO and the CMX994EF minimum filter bandwidth selected. The positive and negative offsets have very similar performance. All results stated are at BER < 1e-2 and the wanted signal level is -104 dBm for the interferer tests.

- Sensitivity ~ -121 dBm
- Adjacent Channel Rejection ~ 57 dB

8.4.1.3. Results with QAM

The following results were all taken with the CMX994EF ACR filter set at its maximum setting and the on-board LO at 896 MHz. The input was at 448 MHz and the baud rate in all cases was 18 ksymbols/s. The plot in Figure 16 compares the sensitivity curves of the three different QAM types.

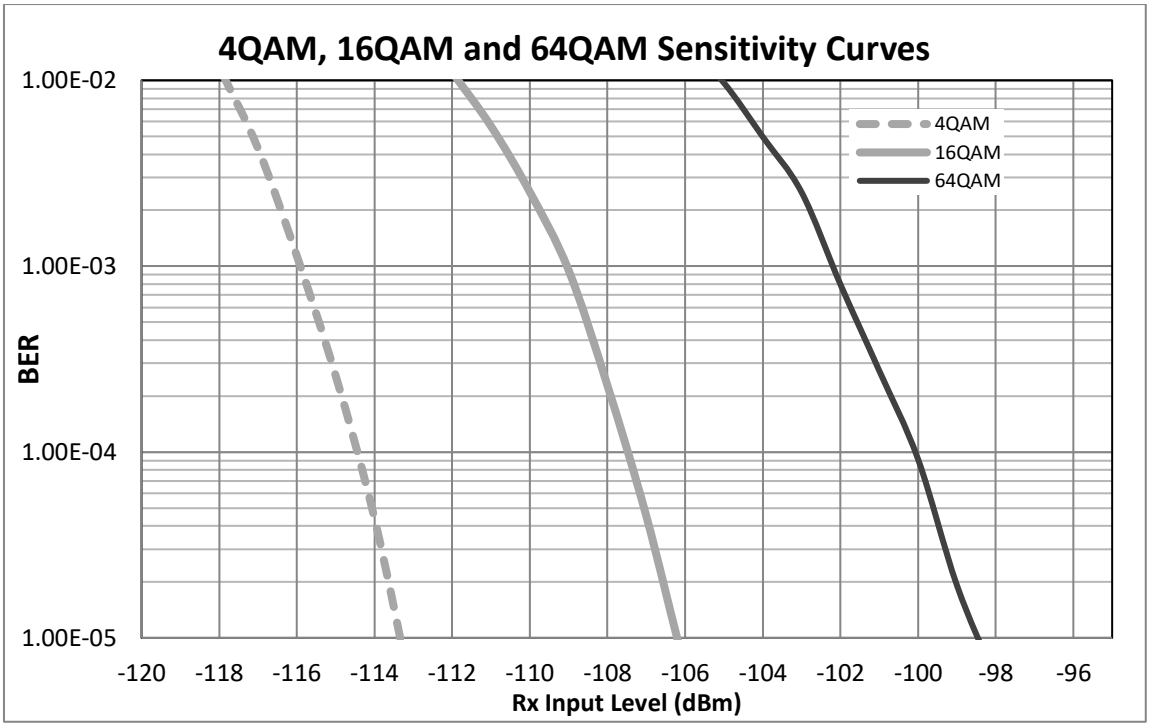


Figure 16 - 4QAM, 16QAM and 64QAM Sensitivity Curves

8.5. Troubleshooting

The CMX994EF is a complex RF system. If incorrectly programmed or modified, results will be at variance from datasheet performance. Please study the IC datasheet, this user manual and the associated schematics and layout drawings carefully when troubleshooting.

This section provides some suggestions to help users resolve application issues they might encounter.

8.5.1. General

Table 11 - Possible General Errors

Error Observed	Possible Cause	Remedy
'**ES9942EFxx.exe**' software fails to run correctly and reports an error during start up.	Faulty USB port or cable.	Check USB cable to your PC.
	PE0003 or EV9942EF is not powered up during start up.	Power up PE0003 (5.0 V) and EV9942EF (7.2 V).
	Incorrect software for PE0003.	Contact: techsupport@cmlmicro.com
Programming data to EV9942EF does not appear to work.	The data is being programmed to the wrong C-BUS port on PE0003.	Check whether EV9942EF is connected to PE0003 Port 1 (J5) or Port 2 (J3) and ensure the correct window is used for programming data. (See PE0003 user manual for further information).

8.5.2. Receiver Operation

Table 12 - Possible Receiver Errors

Error Observed	Possible Cause	Remedy
No output from the receiver.	The receiver has not been enabled by either the RXEN pin or the C-BUS Rx enable ($11, b1).	Set C-BUS Rx enable ($11, b1 = '1') or set RXEN (pin 23) high.
No output from the receiver.	The PCB does not have the LNA connected to the down-converter mixers using C7, C15, C8 etc or filter FL1.	Check hardware configuration and ensure received signal is present at pin 9.
No output from the receiver.	The RF input is connected to the wrong connector. Note: Input is J5.	Check hardware configuration and ensure received signal is present at pin 6.
Adjacent channel performance is not the same on +ve offset and –ve offset.	The VCTCXO control line has not been setup to ensure the PLL frequency is centred on the channel. Note: the default configuration of the EV9942EF is that the control voltage to the VCTCXO is fixed by means of R18 and R21.	Apply a suitable signal to AFC, which can be monitored on TP3.
PLL does not lock. (Lock detect bit = '0').	VCO is not enabled. LO Input is not enabled. M and R Divider setting are incorrect.	Check values of PLL registers $20, $21, $22, $23 and $24.
	VCO has been programmed to a frequency outside its operating range.	Check VCO control voltage on CMX994EF signal DO (pin 20 or TP5). If the voltage is at either supply rail, try a different frequency and observe the effect.

8.5.3. Transmitter and PLL Operation

Table 13 - Possible Transmitter Errors

Error Observed	Possible Cause	Remedy
No output from the transmit LO path.	The transmitter has not been enabled by either the TXEN pin or the C-BUS Tx enable ($11, b0).	Set C-BUS Tx enable ($11, b0 = '1') or set TXEN (pin 22) high.
No output from the transmit LO path.	The wrong Tx divider ratio has been selected ($25, b5 & b6)	Check CMX994EF Datasheet for details on register $25 to ensure correct divider ratio selected.
PLL does not lock. (Lock detect bit = '0').	VCO is not enabled. LO Input is not enabled. M and R Divider setting are incorrect.	Check values of PLL registers $20, $21, $22, $23 and $24.
	VCO has been programmed to a frequency outside its operating range.	Check VCO control voltage on CMX994EF signal DO (pin 20 or TP5). If the voltage is at either supply rail, try a different frequency and observe the effect.

9. Performance Specification

9.1. Electrical Performance

9.1.1. Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the evaluation kit.

	Min.	Max.	Units
Supply Voltage (V_{IN} - V_{SS})	0	8.0	V
Current into or out of VIN and VSS pins	0	+2.0	A
Current into or out of any other connector pin	-20	+20	mA

9.1.2. Operating Limits

Correct operation of the evaluation kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply Voltage (V_{IN} - V_{SS})		5.25	8.0	V

9.1.3. Operating Characteristics

For the following conditions unless otherwise specified: V_{IN} - V_{SS} = 7.2V, Tamb = +25°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (CMX994EF Powersaved)	2, 3	–	16	–	mA
I_{DD} (Rx Enabled, PLL and VCO)	2	–	95	–	mA
I_{DD} (Tx Enabled, PLL and VCO)	2	-	50	-	mA
I_{DD} (Rx Enabled enhanced IP3 mode, PLL and VCO)	2,11	–	103	–	mA
AC Parameters					
Receiver Input					
Input Impedance		–	50	–	Ω
Input Level		–	–	3	dBm
Frequency Range (Default Components)	10	446	448	450	MHz
Frequency Range (With FL1 Fitted)	10		446		MHz
Frequency Range (With External LO)		440		460	MHz
Filter Bandwidth	4	–	2 / 4 / 8	–	kHz
I/Q Output Signal					
Amplitude	5	–	440	–	mVp-p
DC Level		–	1.6	–	Vdc
LO Input (J7)					
Input Impedance		–	50	–	Ω
Frequency Range		100	–	2000	MHz
Input Level		–	-10	–	dBm
Frequency Reference (U2)					
Frequency		–	19.2	–	MHz
Stability		–	1.5	–	ppm
448 MHz Rx Operation					
Gain	7	62.5	63	64.5	dB
Noise Figure		–	4	6	dB
Input Third Order Intercept Point		-4	-2	–	dBm
Enhanced Input Third Order Intercept Point	11	-1	0	–	dBm
Input Second Order Intercept Point	8	45	62	–	dBm
Sensitivity	6	–	-116	–	dBm
Tx Operation					
Output Level	9	-5	-3.5	–	dBm
Frequency Range		100	–	1000	MHz
C-BUS Interface					
See CMX994EF Datasheet					

Notes:

2. Total PCB current consumption, not current consumption of the CMX994EF alone.
3. Current consists of TR2/TR3 VCO (15 mA); VCTCXO (1 mA).
4. Bandwidth is selectable in the CMX994EF IC, see CMX994EF datasheet for details.
5. 448 MHz input at –60 dBm at J5.
6. 4-FSK modulation, 3 kHz deviation, 19 200 bits/s at a BER of $1x10^{-2}$.
7. Gain is measured from RF input (assumed to be 50 Ω source /load) to differential voltage measured at output of I or Q channels.
8. Measured at +1 MHz offset.
9. Measured at 448 MHz.
10. Operating range set by tuning range of 892 MHz VCO.
11. CMX994EF (EV9942EF only) in Enhanced mode ($15, b7='1')

ROHS Compliance

CML Micro certifies, to the best of our knowledge, that its products comply with **RoHS directive (2011/65/EU)**, as amended by **Directive (EU) 2015/863.**

REACH Compliance

CML Micro certifies, to the best of our knowledge, that its products do not contain any of the banned substances specified in the SVHC list at https://echa.europa.eu/candidate-list-table. CML Micro are committed to ensuring the safety of products and the compliance with regulations. Publications will be updated in the event that REACH control is compromised.

Contact information

For further information please contact your local CML sales representative.

Contact details can be found at www.cmlmicro.com

Important notice: The information provided in this document is believed to be accurate and reliable however, CML assumes no responsibility for any errors or omissions in this document. CML reserves the right to make changes to this document at any time without notice.

The product(s) referenced within this document are not designed, authorized, or warranted for use in life support, life-critical, surgical or nuclear applications, nor in any application where the failure of the product could create a situation where personal injury or death may occur. Customers using or selling the product for such applications do so entirely at their own risk and without any recourse to CML, financial or otherwise.

CML assumes no liability for applications assistance or the design of customers' products. Customers are solely responsible for the design, validation, and testing of customer products as well as compliance with all legal, regulatory, and safety-related requirements concerning their applications.

Evaluation kits and demonstration boards are supplied for the sole purpose of demonstrating the operation of CML products and are supplied without warranty. They are intended for use in a laboratory environment only and are not for re-sale, end-use or incorporation into other equipment. Operation of these kits and boards outside a laboratory environment is not permitted within the European Community. All software/firmware is supplied "as is" and is without warranty. It forms part of the product supplied and is licensed for use only with this product, for the purpose of demonstrating the operation of CML products. Whilst all reasonable efforts are made to ensure that software/firmware contained in this product is virus free, CML accepts no responsibility whatsoever for any contamination which results from using this product and the onus for checking that the software/firmware is virus free is placed on the purchaser of this evaluation kit or development board.

ALL SPECIFICATIONS AND DATA ARE PROVIDED "AS IS" AND WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. PRODUCTS ARE PROVIDED UNDER THE TERMS OF CML'S CONDITIONS OF SALE.

Nothing in this document or any purchase of CML products shall be construed as granting any license, whether express or implied, under any patent, copyright, trade secret, or other intellectual property right owned or controlled by CML.