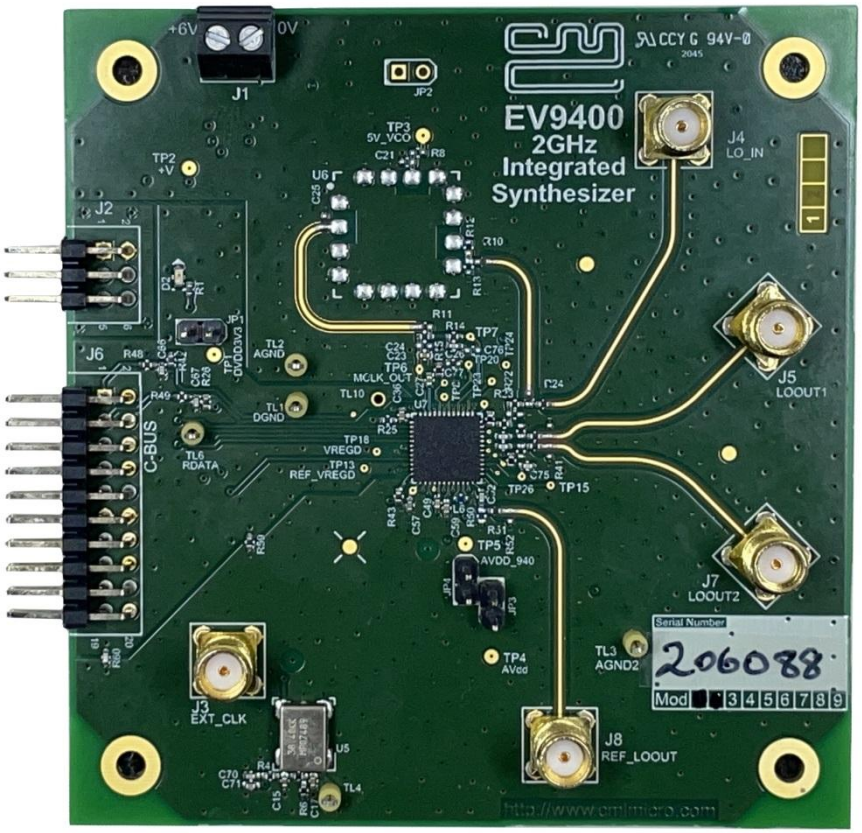
EV9400
Evaluation Kit for CMX940

UM9400/4 November 2020 **USER MANUAL** Advance Information

Features

- **Demonstrates the CMX940 fully integrated Fractional-N RF PLL with reference PLL and VCOs**
- **On-board reference oscillator with options for an external source**
- **Dual RF output for Tx and Rx sub-systems**
- **49 – 2040 MHz continuous output frequency**



1 Brief Description

The EV9400 is a demonstration and evaluation platform for the CMX940 High Performance RF Synthesizer with integrated VCOs. The CMX940 provides a continuous output range of 49 to 2040 MHz, generated using a fully integrated 2720 to 4080 MHz RF VCO with selectable output frequency dividers and 16- or 24-bit Fractional-N PLL. A highly-configurable reference path, consisting of a separate PLL and VCO, can be used to minimise close-in phase noise and mitigate integer and fractional boundary spurious. The reference VCO has a range of 600 – 1200MHz and is set by an external inductor.

The board includes all necessary voltage regulators and is operated from an external ~5.5V dc supply.

The EV9400 provides an on-board 38.4 MHz low-noise reference oscillator along with the option for an external reference input. The EV9400 interfaces to the PE0003 Universal Interface Card to allow read and write access to the CMX940 registers. A graphical user interface (GUI) is available for operational set-up as well as handling control scripts.

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It is recommended that you check for the latest product datasheet version from the Products page of the CML website: www.cmlmicro.com

This is Advance Information; changes and additions may be made to this document. Parameters marked TBD or left blank will be included in later issues of this document. Information in this advance document should not be relied upon for final product design.

2 History

Version	Changes	Date
1	Internal release	March 2019
2	Internal release	April 2019
3	First public release	September 2020
4	Updated following board revision and addition of spur avoidance calculator in the GUI	November 2020

ESD Caution

High-performance RF integrated circuits are highly sensitive to electrostatic discharge (ESD) and may contain unprotected inputs and outputs. Handling and assembly should be conducted in an ESD-controlled environment. It is recommended that ESD precautions and protocols are adopted to minimise the risk of electrostatic discharge and protect product integrity.

3 Block Diagrams

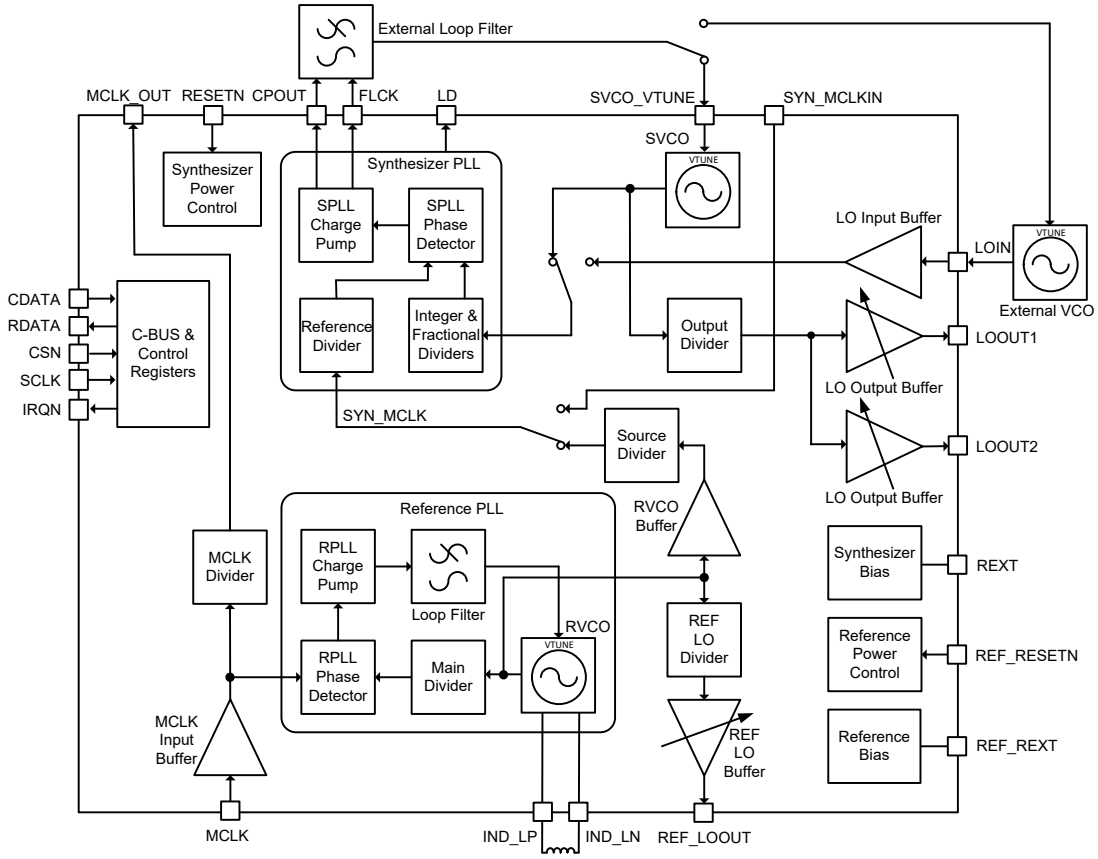


Figure 1 CMX940 Block Diagram

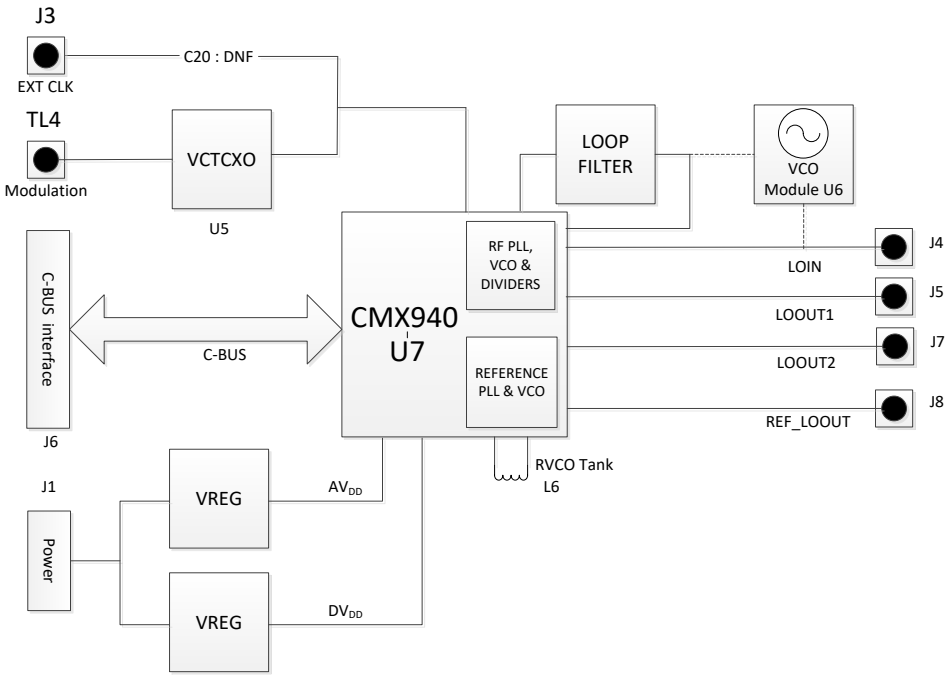


Figure 2 EV9400 Block Diagram

4 Preliminary Information

The EV9400 provides a complete platform for demonstrating and evaluating the CMX940 (device U7). This document refers to revision D of the EV9400.

4.1 Laboratory Equipment

The following items are essential for evaluation of the EV9400:

- Laboratory power supply
- PE0003 Universal Interface Card
- PC
- RF spectrum analyser

For more detailed design or investigation work, additional RF test equipment may be required.

4.1.1 Power Supply

The input voltage to the PCB at J1 is nominally 5.5 V (limits: Minimum 5.25 V to maximum 6.0 V). The input power supply should be rated at 250 mA. On-board regulators provide the 3.3 V and optional 5.0 V VCO module supplies to the circuits used on the PCB. If the VCO module regulator U2 is used, then the input supply must provide sufficient headroom for correct operation.

NOTE: Care should be exercised with the supplies as there is the option to power the EV9400 directly from the PE0003 +5 V supply via J2, although the additional components for this (L2, R2 and R3) are not fitted as standard. If these components are fitted, an external supply should not be connected to J1.

Use of the PE0003 supply is not recommended with a VCO module (and therefore U2) enabled.

4.2 Handling Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation.

4.2.1 SSD Devices

This product uses low-power CMOS circuits that can be damaged by electrostatic discharge. Partially-damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

4.2.2 Contents - Unpacking

Please ensure that you have received all of the items on the separate information sheet (EK9400) and notify CML within seven working days if the delivery is incomplete.

4.3 Approvals

This product is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements, which may apply to this product and the radio frequency signals that may emanate from it.

5 Quick Start

This section provides instructions for users who wish to experiment immediately with this Evaluation Kit. A more complete description of the kit and its uses appears later in this document. The user should also read the CMX940 Datasheet before using the EV9400 board.

NOTES: The default configuration of EV9400 uses the following configuration:

- U5: 38.4 MHz frequency reference.

5.1 Setting-Up

The following procedure is recommended:

1. Connect the boards as shown in Figure 3.
2. Ensure that the power supply and reference oscillator selection links are correctly configured. Refer to Table 6.
3. LO Output signals from the main RF SPLL can be monitored by a spectrum analyser connected to J5 (LOOUT1) or J7 (LOOUT2).
4. Output from the Reference RVCO /PLL can be monitored by a spectrum analyser connected to J8 (REF_LOOUT).
5. Apply power to the boards.

The boards are now ready for operation.

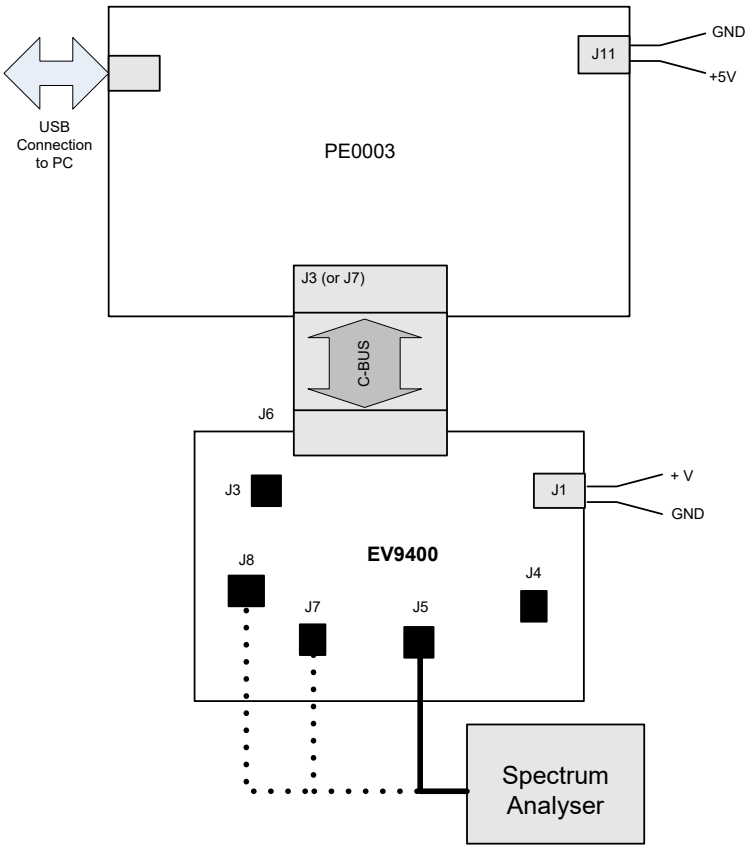


Figure 3 Typical Evaluation Connections for EV9400

5.2 Operation

When power is applied to the EV9400, the CMX940 will be reset.

5.3 Signal Lists

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J1	1	+V	DC	5.5 V Power supply input
J1	2	GNDA	DC	Power supply ground
J4	N/A	LO_IN	RF	Input to the RF PLL (from external VCO)
J7	N/A	LOOUT2	RF	Output from the RF PLL / dividers
J6	-	-	I/P & O/P	C-BUS control connection
J5	N/A	LOOUT1	RF	Output from the RF PLL / dividers
J8	N/A	REF_LOOUT	RF	Output from the RVCO
J3	N/A	EXT_CLK	RF	External PLL reference clock input

Table 1 Connectors

CONNECTOR PINOUT for J6				
Connector Pin No.	**Signal Name**	**Signal Type**	**Description**	
1	REF_RESETN	I/P	Hardware reset for REF PLL	Low to reset, pulled high by R42
2	CSN	O/P	Chip Select	
3	RESETN		Hardware reset for SPLL	Low to reset, pulled high by R26
4	CDATA	O/P	Command Data	
5	N/C		No Connection	
6	SCLK	O/P	Serial Clock	
7	N/C		No Connection	
8	RDATA	I/P	Reply Data	
9	N/C		No Connection	
10	IRQN	I/P	Interrupt Request (open-drain)	
11	GNDD	Power	Connection to Digital Ground	
12	GNDD	Power	Connection to Digital Ground	
13 to 20	N/C		No Connection	

Table 2 External C-BUS Host Interface

CONNECTOR PINOUT for J2			
Connector Pin No.	**Signal Name**	**Signal Type**	**Description**
A/1	DGND_PE0003	Power	Connection to Digital Ground for PE0003
B/2	DGND_PE0003	Power	Connection to Digital Ground for PE0003
C/3	+5V_PE0003	Power	Connection to +5 V supply from PE0003
D/4	+5V_PE0003	Power	Connection to +5 V supply from PE0003
E/5	+5V_PE0003	Power	Connection to +5 V supply from PE0003
F/6	+5V_PE0003	Power	Connection to +5 V supply from PE0003

Table 3 Optional PE0003 Host / Interface DC connector

TEST POINTS		
Test Point Ref.	**Typical Measurement**	**Description**
TP1	3.3 V	U1 Regulator Output (DVDD3V3) for digital supplies
TP2	5.5 V	+V Input supply voltage
TP3	5.0 V	U2 (not fitted) Regulator Output (5V VCO) for the optional VCO module U5
TP4	3.3 V	U3 Regulator Output (AVDD) for analogue supplies to VCTCXO
TP5	3.3 V	U3 Regulator Output (AVDD_940) for analogue supplies to CMX940
TP6	-	CPOUT – SPLL Charge pump output voltage (pin 46)
TP7	-	SVCO_VTUNE Voltage (pin 40)
TP8	1.8 V	VREG_DIV voltage (pin 43)
TP9	-	TEST – No user function
TP10	-	Not assigned
TP11	1.19 V	REXT reference voltage (pin 30)
TP12	1.19 V	REF_REXT voltage (pin 28)
TP13	1.8 V	REF_VREGD decoupling voltage (pin 11)
TP14	1.9 V	RVCO_DEC2 voltage (pin 26)
TP15	-V	RVCO_TUNE (pin 25)
TP16	3.3 V	VDD_LO (pin 34)
TP17	1.8 V	VREG_LO decoupling voltage (pin 32)
TP18	1.8 V	VREGD decoupling voltage (pin 8)
TP19	-	Not assigned
TP20	-	LD, Lock Detect output (pin 42)
TP21	1.8 V	VREG_CLK decoupling voltage (pin 13)
TP22	1.8 V	REF_VREG_CLK decoupling voltage (pin 16)
TP23	2.3 V	SVCO_DEC1 decoupling voltage (pin 36)
TP24	1.0 V	SVCO_DEC2 decoupling voltage (pin 41)
TP25	-	FLCK (pin 44)
TP26	1.2 V	RVCO_DEC1 voltage (pin 27)

Table 4 Test Points

TEST LOOPS		
Test Loop Ref.	**Default Measurement**	**Description**
TL1	DGND	Connection to Digital Ground
TL2	AGND	Connection to Analogue Ground
TL3	AGND	Connection to Analogue Ground
TL4		Modulation Input for VCTCXO (U5)
TL5		Not assigned
TL6		RDATA
TL7		Not assigned
TL8		Not assigned
TL9		Not assigned
TL10		MCLK_OUT (pin 48 – if function activated)

Table 5 Test Loops

JUMPERS		
Ref.	**Default Setting**	**Description**
JP1	Linked	DVDD – Link to enable CMX940 digital supplies.
JP2	Not Fitted	5 V Analogue Supply - Link to enable the optional VCO Module supply
JP3	Linked	AVDD – Analogue Supply - Link to enable VCTCXO supplies
JP4	Linked	AVDD_940 – Link to enable CMX940 analogue supplies

Table 6 Jumpers

Notes:

I/P	=	Input
O/P	=	Output
TL	=	Test Loop
TP	=	Test Point

6 Circuit Schematics and Board Layouts

For clarity, the circuit schematic diagrams are available as separate high-resolution files, which can be downloaded from the CML website. The layout on each side of the PCB is shown in Figure 4 and Figure 5.

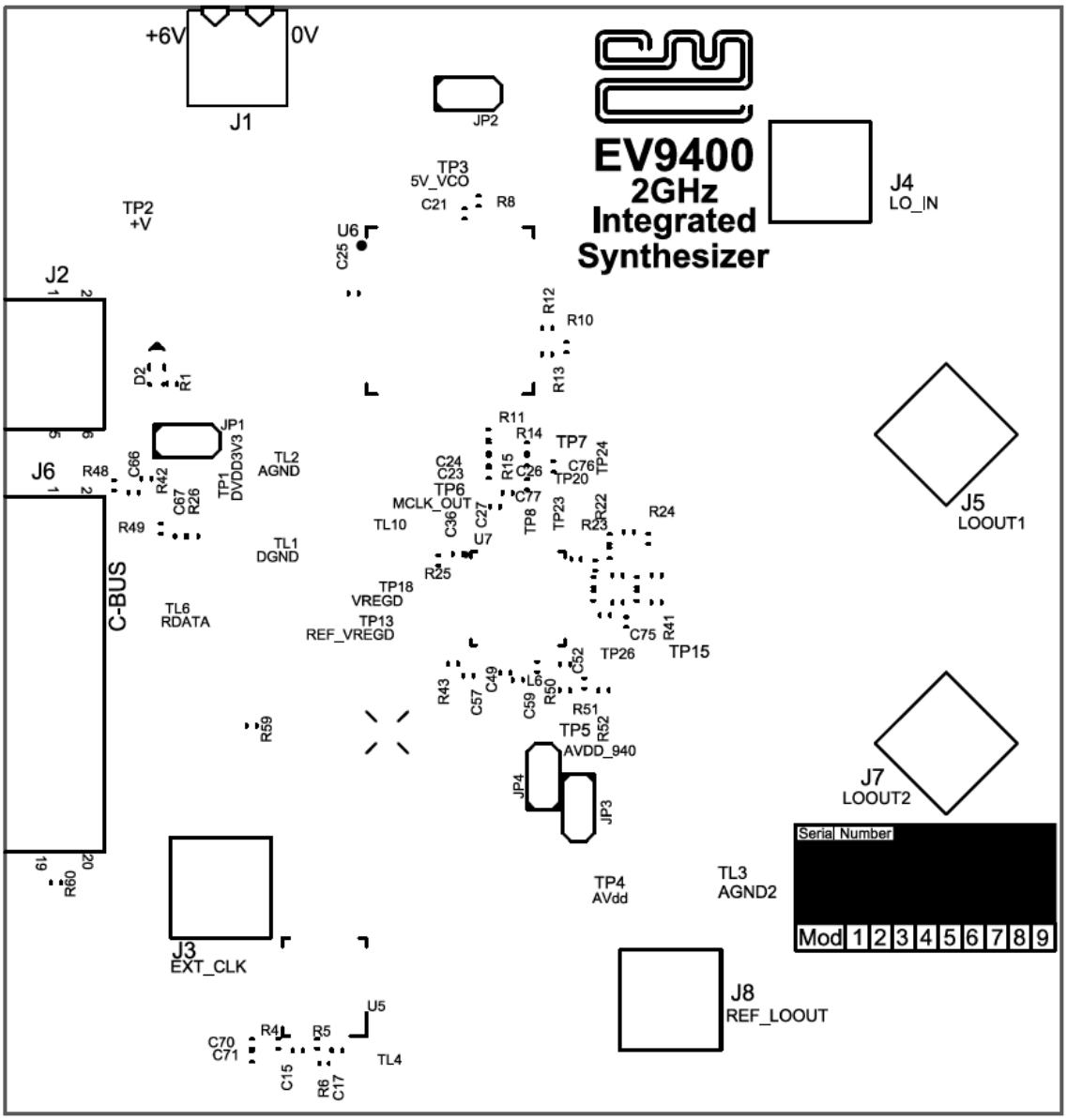


Figure 4 PCB Layout: Top

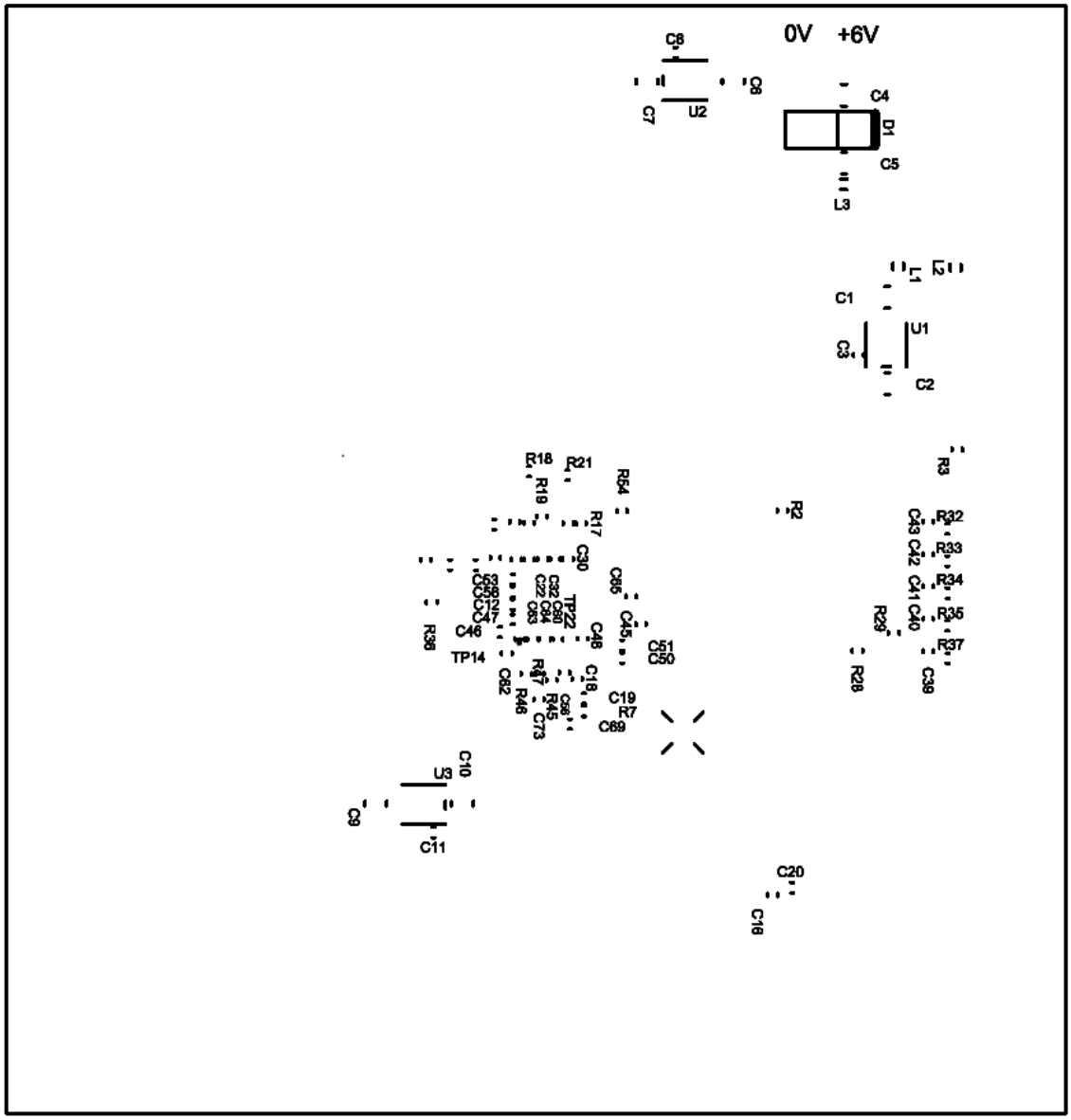


Figure 5 PCB Layout: Bottom

7 Detailed Description

The EV9400 serves as a demonstrator for the CMX940, a 48-contact LGA (Land Grid Array) device at location U7. EV9400 functionality includes:

- 49 to 2040 MHz outputs from the on-chip 16 / 24-bit Fractional-N PLL
- Reference PLL and VCO centred at 960 MHz
- 38.4 MHz clock reference VCTCXO or external reference input
- USB Interface via a PE0003 to a CML GUI, to allow script control

7.1 Hardware Description

Full details of the silicon functionality are contained in the CMX940 Datasheet. The EV9400 is assembled on a 83 x 87mm, 1.6mm thick 4-layer PCB (reference PCB775C), using FR4 / VT481 2116 dielectric.

In general, RF components, connectors and configuration links have been placed on the top layer, with voltage regulators, supplies and decoupling for the CMX940 on the bottom layer. The layout has been optimised for low ground impedance and short RF tracking for operation at high frequencies. Gerber files and a BOM can be downloaded from the CML website.

7.1.1 RF Synthesizer PLL / VCO (SPLL)

The CMX940 contains a 16- or 24-bit Fractional-N PLL synthesizer used with on-chip 2720 – 4080 MHz VCO. The loop filter is external to the IC (Figure 6). When using the internal VCO the loop filter needs to be referenced to the same supply as the VCO to achieve the best phase noise performance. This is the configuration on the EV9400. The loop filter output is then routed back to the tuning input of the internal VCO.

A broad tuning range with relatively low tuning sensitivity is achieved by using an automatic frequency calibration routine internal to the IC.

The on-chip VCO is followed by a programmable divider (2, 3, 4, 6, 8, 12, 16, 20, 28, 40 or 56) to provide 49 to 2040 MHz continuous range at J5 or J7 RF outputs.

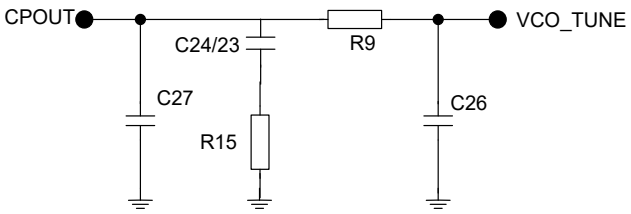


Figure 6 Example External Components – Loop Filter Values

Note: C27, C24/23, R9 and C26 assume a Kvco=40 MHz/V, Icp=1600 µA and FComp=120 MHz from the Reference PLL. The values fitted are a compromise for mid-band operation and give a loop bandwidth around 100 kHz. These values may require modification for use with other comparison frequencies and charge pump currents in order to optimise the phase noise profile. Please refer to the relevant section of the CMX940 Datasheet. The loop filter is referenced to the positive supply via R19 for use with the internal VCO. There is provision for an additional pole at the loop filter output (R14 and C76) but this is not implemented by default.

VCO Frequency	C27	C24/23	C26	R15	R9	R14	C76
3.4 GHz	560 pF	10 nF	33 pF	560 Ω	2.2 kΩ	0 Ω	DNF

Table 7 3rd Order Loop Filter Values for a VCO Frequency of 3.4 GHz

7.1.2 External (off-chip) VCO Use

There are options on the PCB to allow configuration with a VCO module (standard 0.5 inch square footprint) at U6. As a wide variety of frequencies may be required, this is not populated as default. If this or an off-board VCO is to be used, the loop filter components should be reference to ground via R20 (not fitted). There is provision for the output from the VCO module to be attenuated and applied to a resistive splitter before feedback to the CMX940 LOIN pin or monitoring via J4. As default, the LOIN path is configured as a straight through, terminated connection from J4 to LOIN.

The VCO module has a dedicated linear regulator (U2) to provide it with a clean +5.0 V supply. This is not fitted as default to allow for a lower PCB supply voltage (J1) to be accommodated if required.

An external VCO can use the fast lock function, with resistor R21 applied. This is placed in parallel with the R15 value for the duration of the fast lock period.

To use an off-board VCO, the tuning voltage could be taken off-board after R9 and the RF feedback connected to J4. The loop filter also needs to be referenced to ground using a 0R link at C77.

7.1.3 Reference PLL / VCO (REFPLL)

The CMX940 incorporates a low noise reference Integer-N PLL and VCO with internal loop filter. The VCO is tuned by external inductor L6; with the default value fitted the tuning range is centred around 960 MHz. The REFVCO divided output (REF_LO_OUT) is available to monitor at the SMA connector J8. The RVCO is then divided down internally via the Source Divider and used as the reference for the main SPLL.

7.1.4 Reference Oscillator

U5 is a low phase noise GTXO-74V/JI 38.4 MHz VCTCXO reference, part number MP07489, supplied by Golledge (www.golledge.com). This is used as the reference (MCLK) for the REF_PLL and subsequently the SPLL within the CMX940. Options are provided to use an external reference signal applied to the SMA connector J3. The selection of this is via the removal and fitting of C16 and C20 as appropriate. The VCTCXO tuning / adjust input can be accessed via test loop TL4, to allow the addition of a modulating signal within the PLL bandwidth. Applying modulation here may necessitate the removal of the bias network R5, R6 and the removal of the decoupling capacitor C17.

7.1.5 Power Supplies

The input to the PCB is nominally 5.5 V (absolute limits: 5.25 V to 6.0 V) applied to J1. Reverse polarity protection is provided by D1. On-board regulators are provided to generate the 3.3 V and optional 5.0 V supply used on the EV9400. A green LED on the digital supply (D2) confirms that power is correctly applied.

7.1.6 Reset

The Chip Enable inputs (CMX940 pins 29 and 47) are routed to the C-BUS interface. This is active high but can be used to hold the pin low momentarily at power-up to provide a reset function via the GUI or script.

7.1.7 Inductors

All inductors used in the RF sections of the design are manufactured by Coilcraft (www.coilcraft.com). Performance of the circuits with inductors from other manufacturers may vary.

7.2 Adjustments and Controls

The only user hardware control on the board is the ability to select the on-board reference oscillator (U5) or an external source. This is described in section 7.1.4. All other control is via C-BUS and the GUI described in the next section.

7.3 Script/GUI Control

To investigate the performance and features of the EV9400 in more detail, a Windows GUI can be used to control the CMX940 via a PE0003 controller – either by manual register entry or by running scripts. The GUI can be found in 'ES9400xx.zip'.

Setting-Up

- Copy the file 'ES9400xx.zip', which is downloaded from the CML website following registration, to the hard drive of your host PC.
- Extract the files to the hard drive of your host PC.
- Connect a dc supply to the PE0003 Universal Interface Card and set supply voltage level to 5V / 500 mA current limit.
- Connect a dc supply to the EV9400 and set the voltage level to 5.5 V / 250 mA current limit.
- Attach a USB cable between the PE0003 Universal Interface Card and the USB port of the PC.
- Turn on the power supplies.

Install the USB driver when requested. The driver is in the same folder as the 'ES9400xx.zip' files were extracted to (..\Driver). Follow instructions on the screen to install the USB driver. Select the 'Install this driver software anyway' option when the Message Box below is displayed:

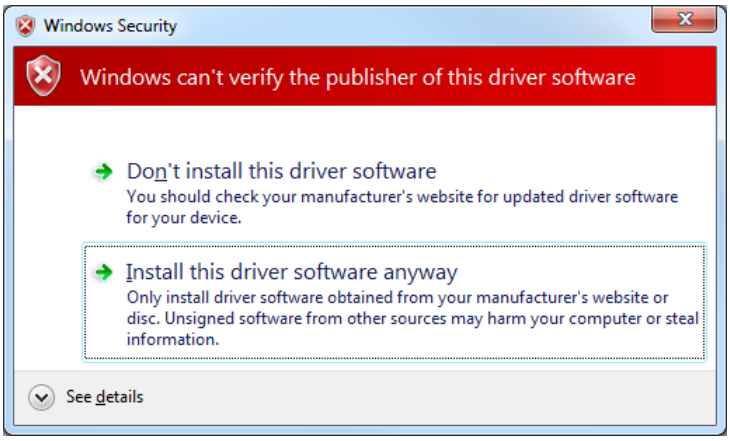


Figure 7 Driver Verification Dialogue

The executable ES9400xx.EXE can now be run.

At the top of the GUI window it is possible to open and save setup files for the GUI and set the C-BUS port (1 or 2) and speed. If the Auto Write tick box is checked all changes made in the GUI will be written immediately, if this is not checked the user must use the "Write All" button on the Master Control tab to ensure that all registers have been configured properly. There are five sheets within the tabbed dialog box structure. These are described in the following sections.

7.3.1 Master Control Tab

This tab provides access to all the user-configurable registers in one place and also provides the critical read back status of the REFPLL and SPLL. For example in the SYNISR_RD box the user will see a blue indicator against the SPLL_CAL if a successful calibration has been performed on the SPLL VCO. Note that the state of the registers in this tab will be updated if the user makes changes to the REFPLL or SPLL via their own individual tabs.

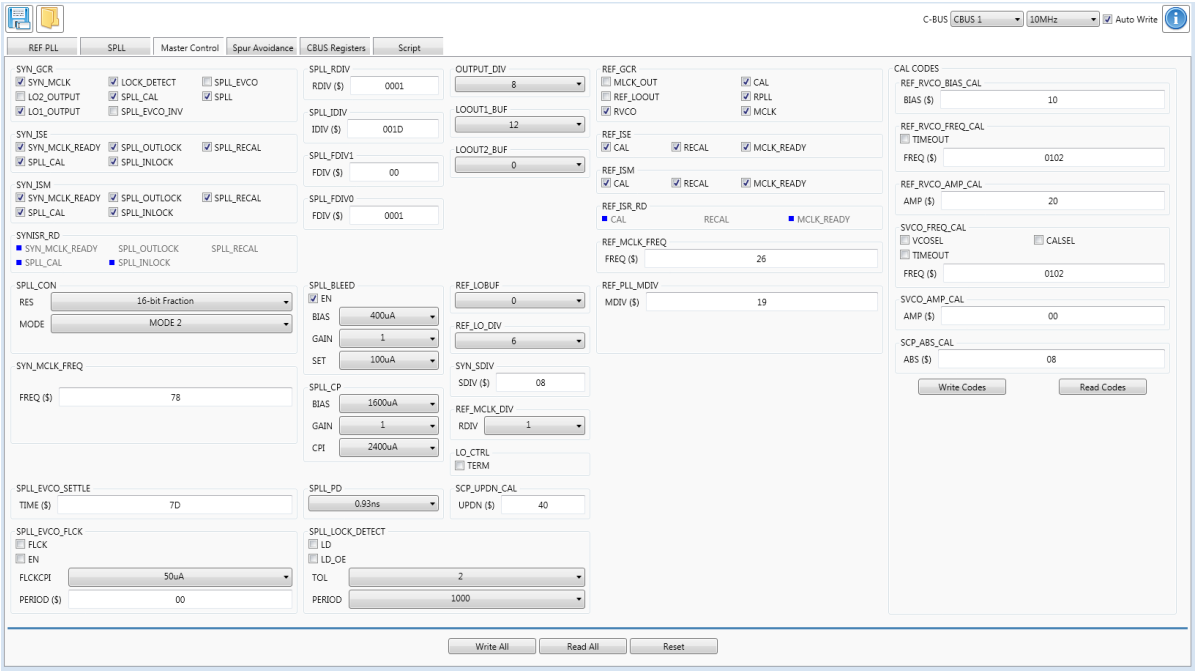


Figure 8 Master Control Tab

7.3.2 REFPLL Tab

The REFPLL as shown in Figure 9 displays the REFPLL diagrammatically and within the block diagram the user can configure the input reference frequency (38.4 MHz), the source divider value (SDIV) and the PLL divider value (MDIV). The "Set Freq" button can be used to enter the RVCO frequency (default 960 MHz) and the MDIV will calculated automatically. There is a drop down menu which allows the user to select the external VCO inductor that is fitted, the default value of the EV9400 is 4.7 nH and details about the frequency coverage of the VCO with this inductor value can be found in the CMX940 Datasheet (refer to the table showing Typical RVCO Centre Frequency). The "En LO Out" button enables the REF LOOUT path, comprising a separate output divider (ODIV) and a buffer. The user will know when this path is enabled as it will appear on the diagram as shown in Figure 10. The "Mclk Out" button enables the MCLKOUT which is a divider (1, 2, 3 or 4) and, when enabled, it will appear as shown in Figure 11.

The status bits for the REFPLL are also shown and if a blue marker appears against them this indicates that the status bit is set. The "CAL" status bit indicates REFPLL calibration complete, "RECAL" indicates when a recalibration of the REF VCO is required and "MCLK_READY" indicates when a suitable MCLK signal is ready. The "Run/Stop" buttons will run or stop a VCO calibration and "Recal" will perform a re-calibration of the VCO. If the "Automatic Recalibration" check box is ticked the REFPLL will recalibrate when necessary.

The "Read Status" button will update the status conditions. The "Reset" button will reset the GUI back to defaults on the REF PLL and SPLL tabs.

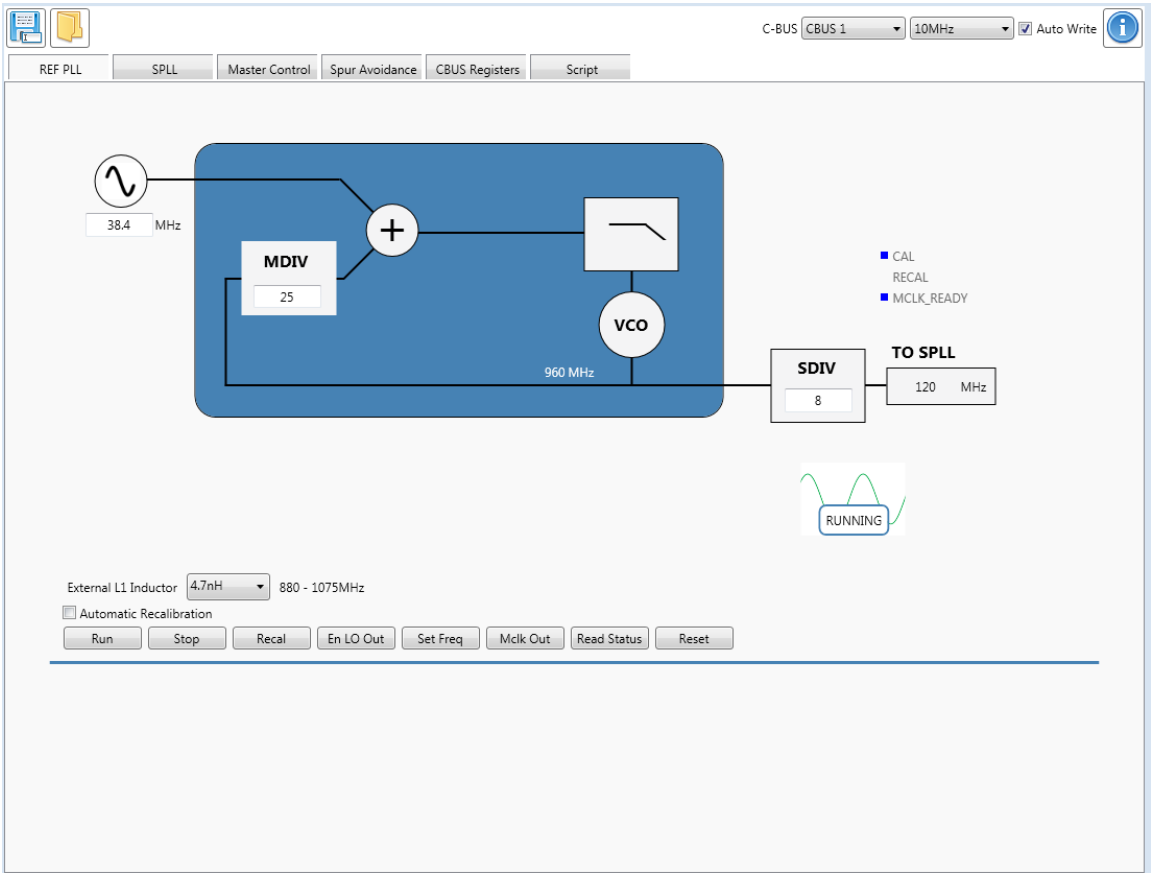


Figure 9 REFPLL Tab

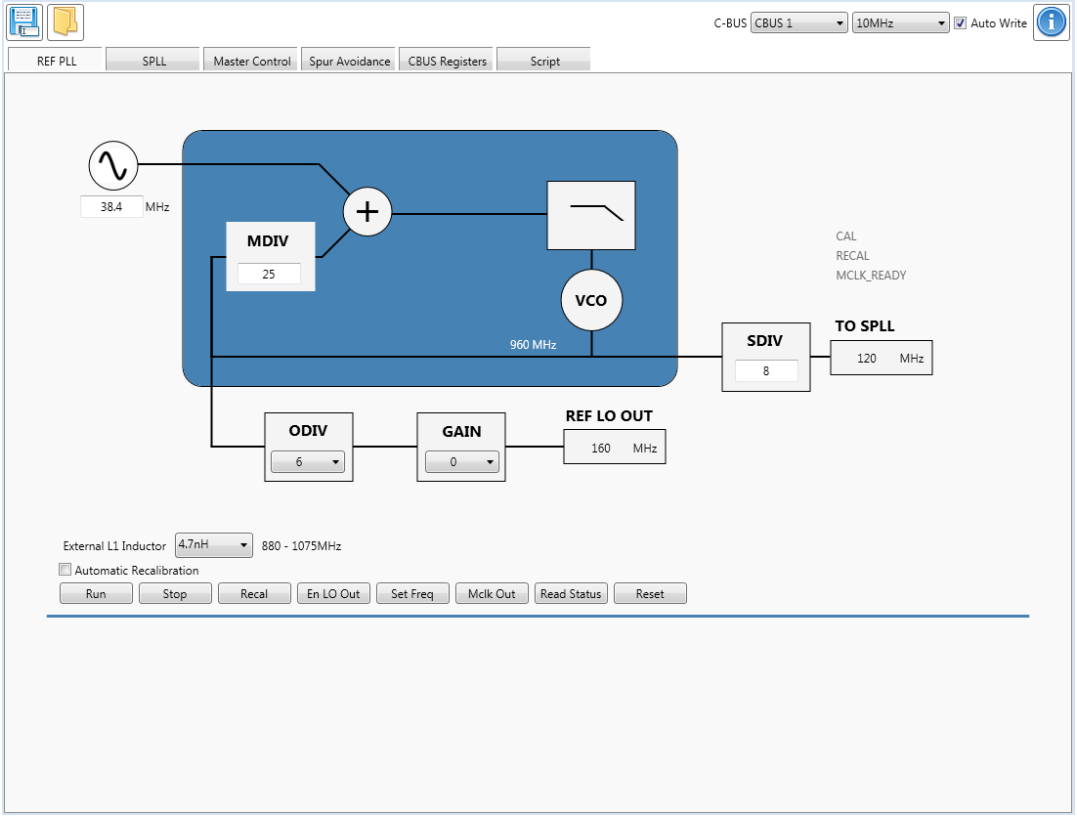


Figure 10 REFPLL Tab Including REF_LOOUT Path

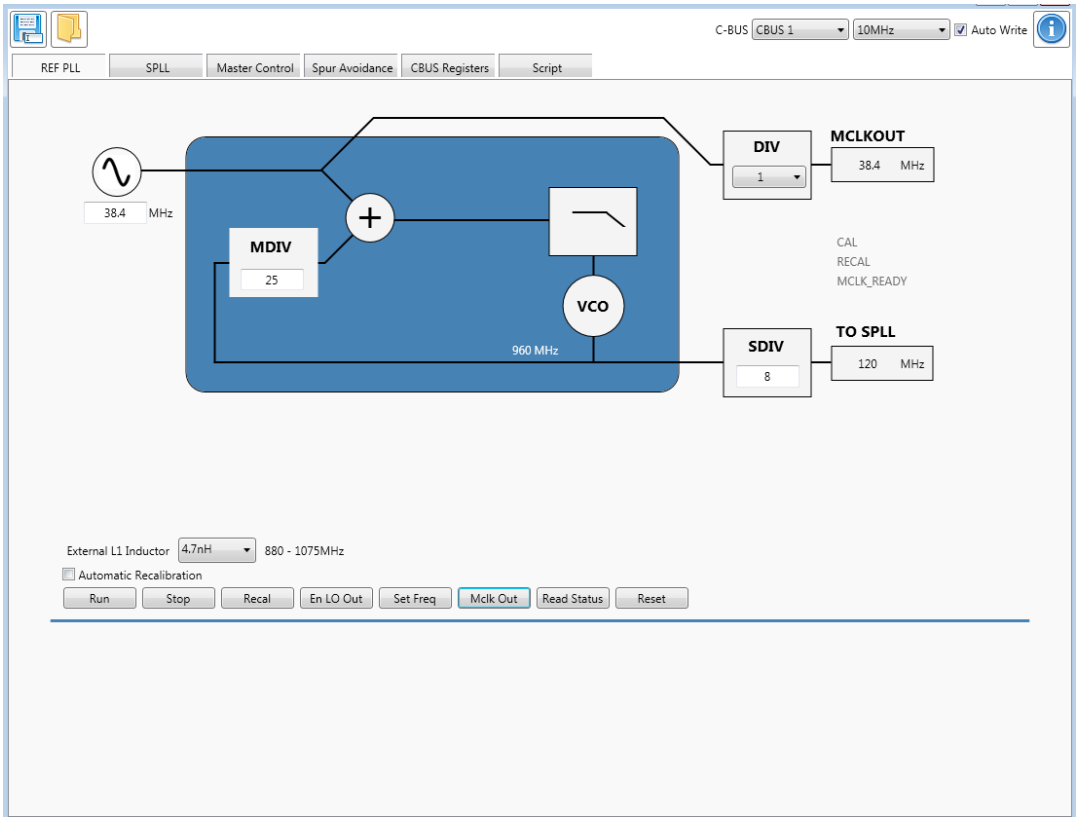


Figure 11 REFPLL Tab Including MCLKOUT Path

7.3.3 SPLL Tab

The SPLL Tab as shown in Figure 12 displays the SPLL diagrammatically and within the block diagram the user can specify the RDIV, the IDIV and the FDIV divider values. The “VCO Freq” button can be used to enter the SVCO frequency (default 3484.2022 MHz) and the “LO Out Freq” (default 435.525 MHz) button can be used to enter the LOOUT1/LOOUT2 output frequency, divider values will be calculated automatically from these entered values. The “En LOUT1/En LOOUT2” button enables the LOOUT path independently which is a separate output divider and buffer in each path. The user will know when these paths are enabled as they will appear on the diagram; Figure 12 shows the LOOUT1 path for example. Drop down menus in this path allow the user to select the divider value and the output gain level.

The status bits for the SPLL are also shown and if a blue marker appears against them this indicates that the status bit is set. The “SYN_MCLK” status bit indicates suitable MCLK is ready, the “SPLL_CAL” status bit indicates the SPLL calibration complete, “SPLL_OUTLOCK” indicates when the SPLL is out of lock, “SPLL_INLOCK” indicates when the SPLL is in lock and “SPLL_RECAL” indicates when a recalibration of the SPLL is required. The “Run/Stop” button will run or stop a VCO calibration and “Recal” will perform a re-calibration of the VCO. If the “Automatic Recalibration” checkbox is ticked the SPLL will recalibrate when necessary.

It is recommended to have “Round Values” and “SPLL Optimisation” ticked as this provides automatic calculation of all the critical loop parameters. “Locked SVCO Freq with RPLL Changes” allows the user to vary the incoming REFPLL frequency but maintain the SVCO frequency so that the resultant output frequency can be maintained. This allows the user to analyse the spur avoidance techniques that can be easily utilised with the CMX940; see section 7.4 of the CMX940 Datasheet.

The drop down menus at the bottom of the screen allow the user to:

- Select the mode of the SPLL; integer or fractional
- 16- or 24-bit fractional mode
- Adjust all SPLL bleed current parameters
- Adjust all charge pump parameters
- Adjust the SPLL minimum pulse width

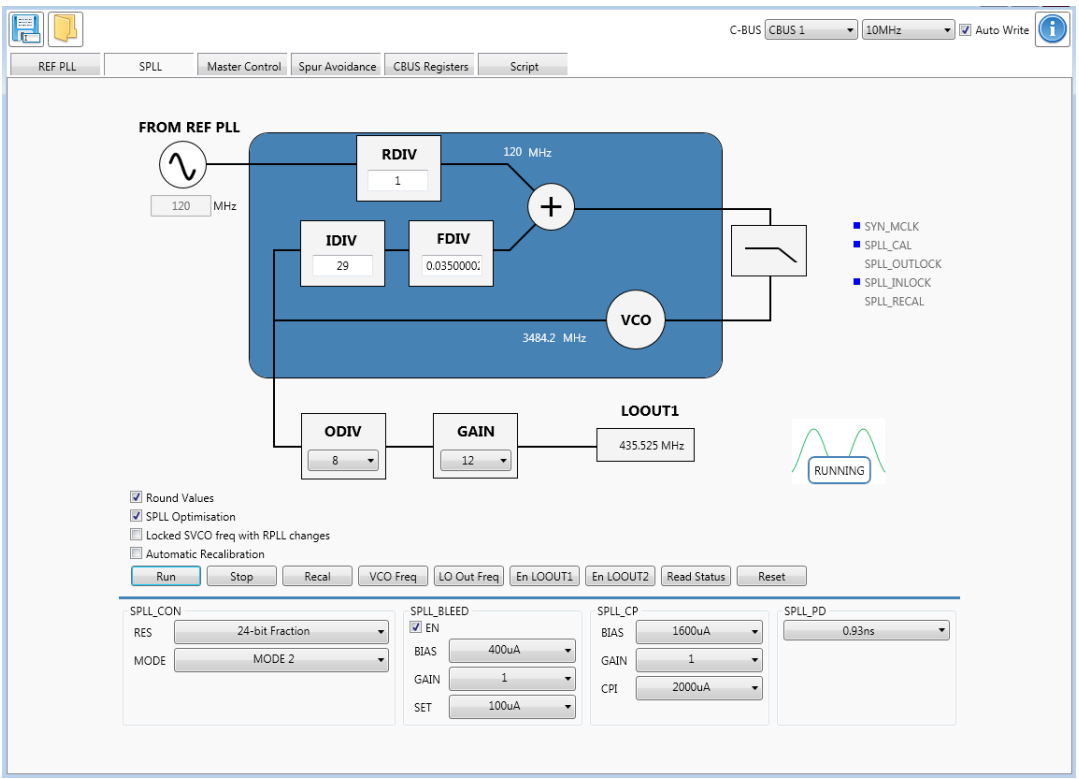


Figure 12 SPLL Tab

7.3.4 Spur Avoidance Tab

This tab provides the user with a quick and easy way to calculate a new set of register values to avoid typical spur scenarios. The calculator will avoid boundary spurs, clock and RVCO spurs (for further information on the calculator see the Spur Avoidance Algorithm application note). This tab enables the user to easily experience the power of the CMX940 spur mitigation mechanism. The user can input the target output frequency and the in-built calculator will determine the correct settings to avoid the typical known spurs by pressing “Calculate”. The new register settings can then be written to the device by pressing “Write Registers”. This also updates the ‘REF_PLL’, ‘SPLL’ and ‘Master Control’ Tabs with the new register values.

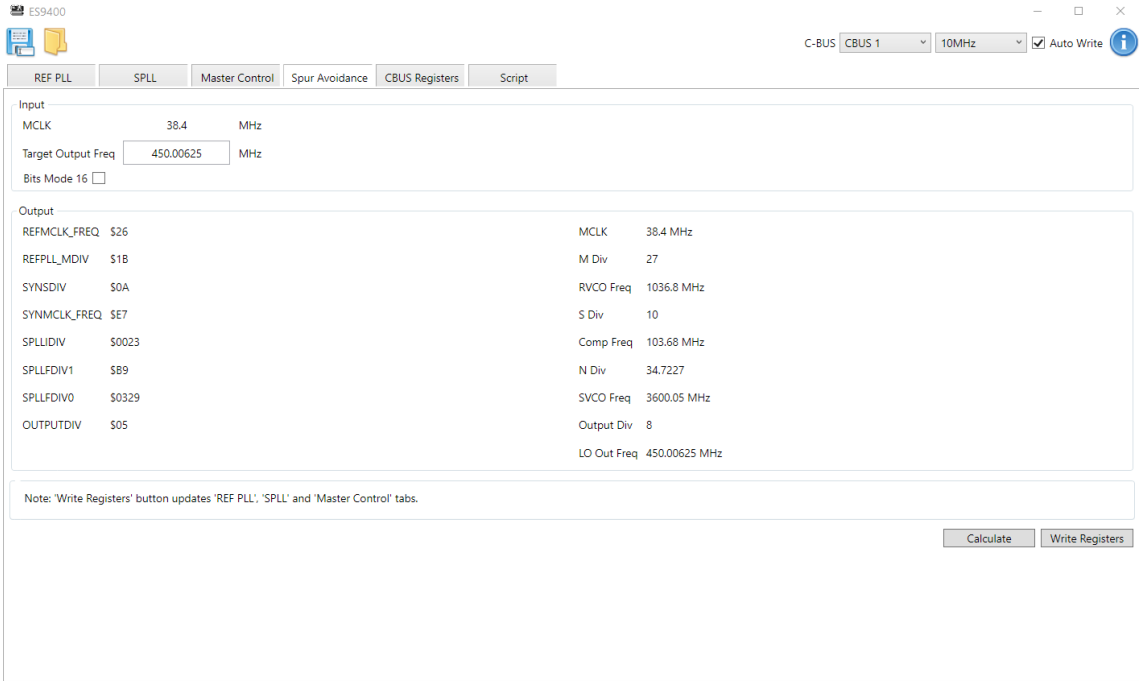


Figure 13 Spur Avoidance Tab

7.3.5 C-BUS Register Tab

This tab provides basic C-BUS read, write and general reset functions; see the left hand section of Figure 14 below.

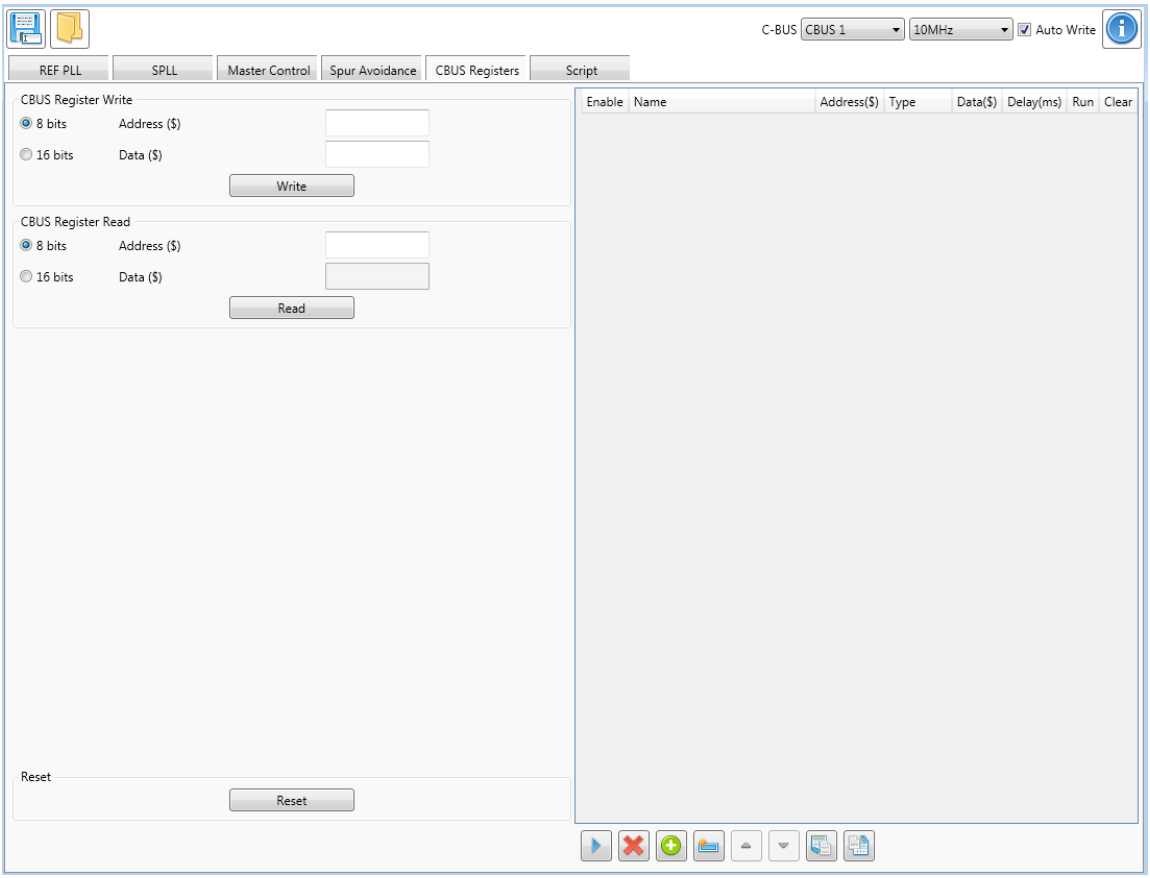


Figure 14 C-BUS Register Tab

Also within this tab users can create their own multiple C-BUS read and write functions, see Figure 15. Each row in the table represents a single write or read action to/from a C-BUS register. The buttons at the bottom right provide the following functions to use this facility:

- Press this to write all enabled C-BUS commands in the user defined list
- Clears all commands in the user list
- Add a “New Register” command line to the list for user to complete
- Add a predefined register command line to the list
- Save/Recall user register list to or from a configuration file

Each line in the register list can be edited by the user and each command can be written individually.

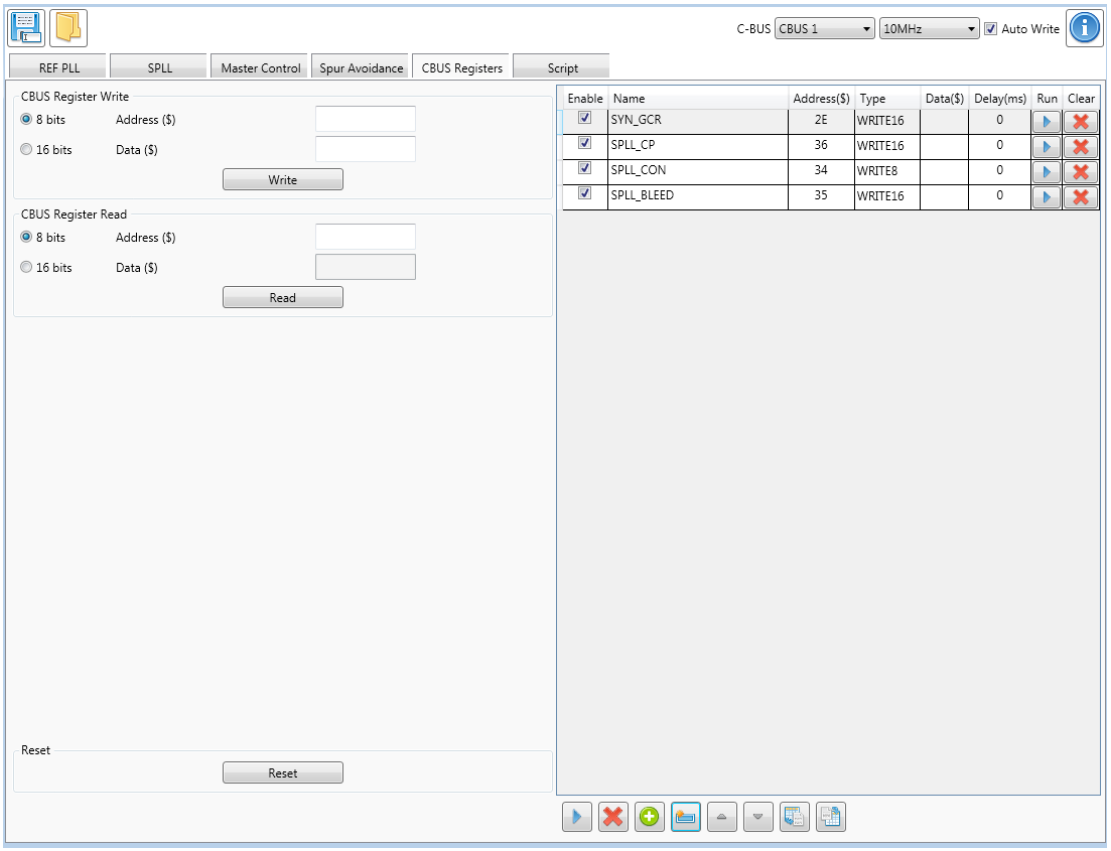


Figure 15 C-BUS Register Tab Simple Multiple C-BUS List

7.3.6 The Script Handler Tab

The Script Handler tab allows the execution of scripts. These are plain text files on the host PC which are compiled by the GUI, but executed on the ARM Microprocessor on the PE0003. The script language is documented separately in the "Script Language Reference" document, which can be downloaded with the PE0003 support package from the CML website at www.cmlmicro.com. The following are demonstration scripts developed for the EV9400 Evaluation Kit:

EV9400_DS01_REFPLL_998M4.pes
This script locks the REFPLL only at 998.4 MHz using the on-board 38.4 MHz VCTCXO as a reference. VCO calibrations are performed and the results displayed. The buffered output is available at REF_LOOUT (J8).

EV9400_DS03_500M Cascade_FracN_24bit.pes
This script locks the REFPLL at 921.6 MHz and the SPLL at 4000 MHz using a 16-bit Fractional-N mode with the output at 500 MHz (divide by 8 output enabled). The comparison frequency is 115.2 MHz. A 2000µA charge pump current is set. RVCO and SVCO calibrations are performed and the results displayed. For additional confidence, the ISR read register is also read back. The output is at LOOUT1 (J5).

EV9400_DS04A_419M9 SpurAvoid1.pes
This is a modified version of DS03 using both the REFPLL at 960 MHz and the SPLL very close to the N=28 boundary (x120 MHz SPLL reference) 3359.9 MHz using a 16-bit Fractional-N mode with the output at 419.9875 MHz (divide by 8 output enabled). RVCO and SVCO calibrations are performed and the results displayed. For additional confidence, the ISR read register is also read back. The output is at LOOUT1 (J5). Spurious at 100 and 200 kHz offsets can be seen.

EV9400_DS04B_419M9 SpurAvoid2.pes
This is a modified version of the above using both the REF_PLL at 1036.8 MHz and the SPLL (using a 115.2 MHz reference), at 3359.9 MHz using a 16-bit Fractional-N mode with the output at 419.9875 MHz (divide by 8 output enabled). RVCO and SVCO calibrations are performed and the results displayed. For additional confidence, the ISR read register is also read back. The output is at LOOUT1 (J5). The previously seen spurious at 100 and 200 kHz offsets are not present.

EV9400_DS05_435M525.pes Cascade_FracN_16bit.pes
This is a modified version of the DS03 script above using both the REF_PLL at 921.6 MHz and the SPLL (using a 115.2 MHz reference), at 3484.2 MHz using a 16-bit Fractional-N mode with the output at 435.525 MHz (divide by 8 output enabled). RVCO and SVCO calibrations are performed and the results displayed. For additional confidence, the ISR read register is also read back. The output is at LOOUT1 (J5).

To select a script file, click on the "Select Script" button. The Open File Dialog is displayed. Browse and select the script file. The folder that contains the script file will be the working folder of the script (i.e. all the files referenced in the script will be searched in this folder).

The results window displays the values returned by the script. These results can be saved to a text file or discarded by clicking on the "Save Results" or "Clear Results" buttons, respectively. When a script file is being executed, the "Run Script" button will change to be the "Stop" button, the rest of the tab will be disabled and the other tabs cannot be selected.

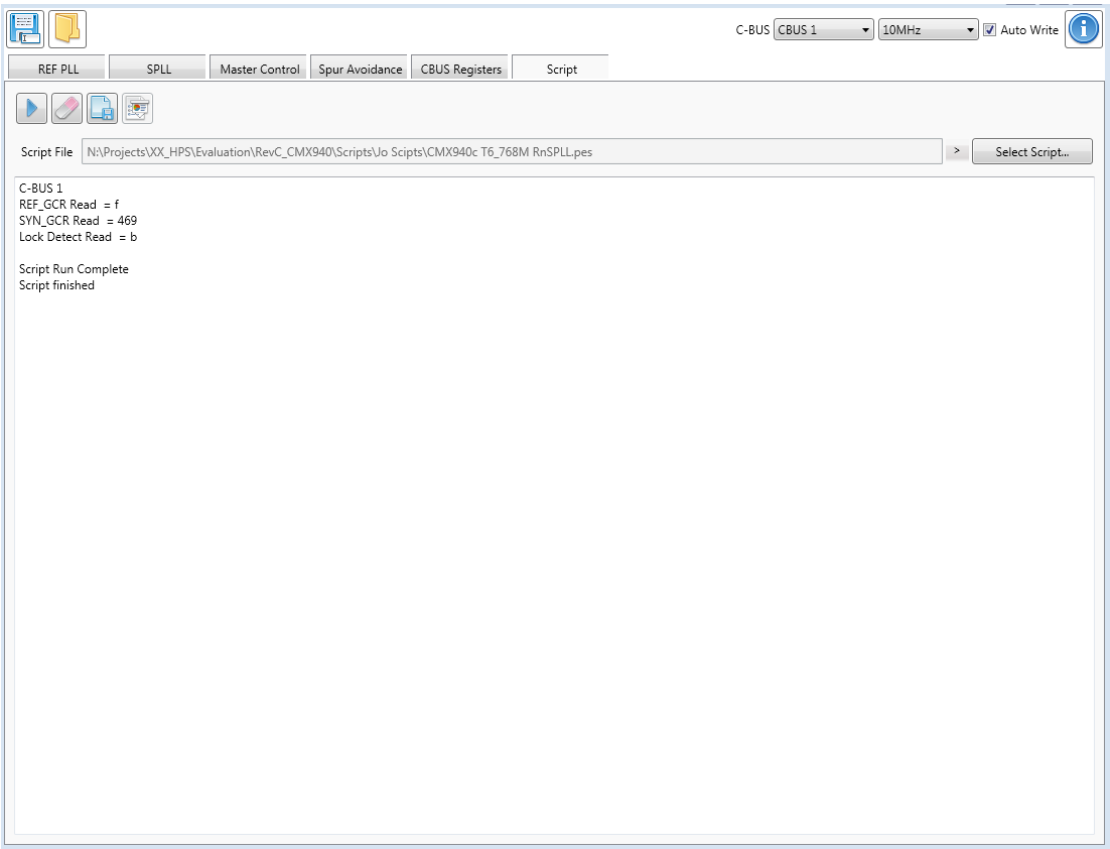


Figure 16 Script Handler Tab

7.4 Application Information

See Section 5.1 for board setup details and Section 5.2 for operation of the EV9400.

7.4.1 Typical Performance

Typical performance for the EV9400 is shown below.

The phase noise profiles can be varied by a number of settings, notably the loop filter bandwidth, comparison frequency, charge pump current, reference noise, output level and divider setting etc.

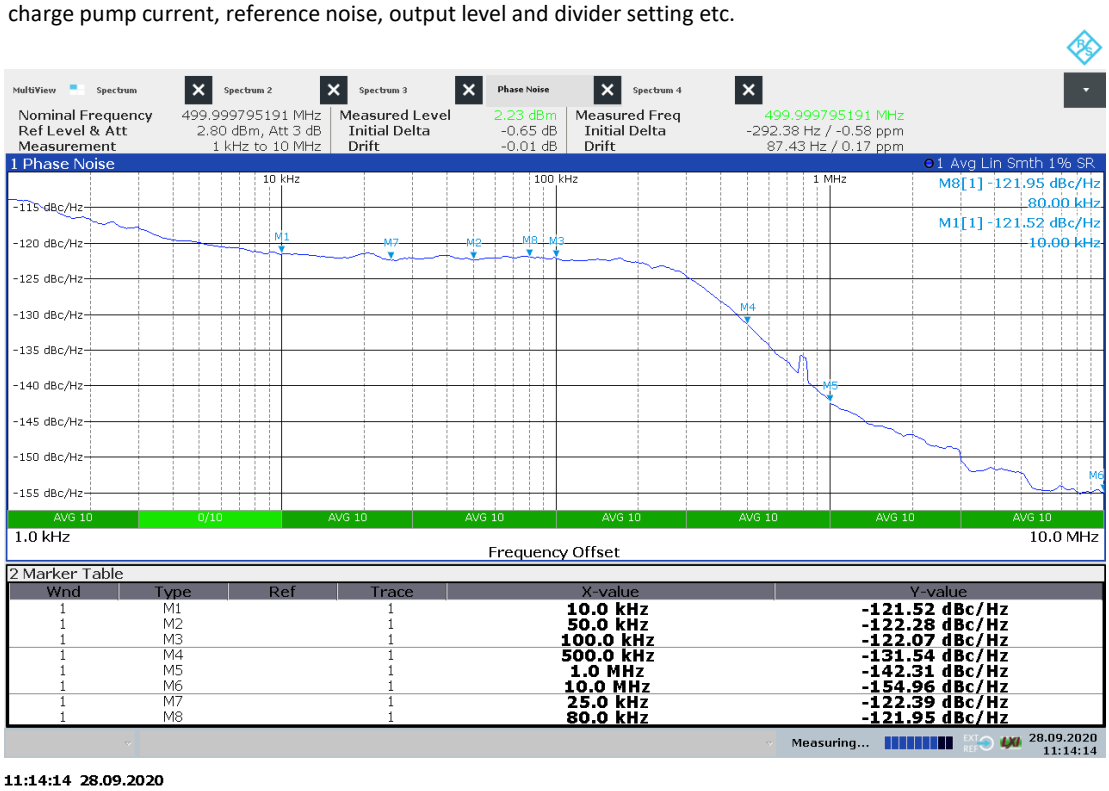


Figure 17 Phase Noise at 500 MHz RF Output

Note: conditions for above plot:
REFPLL = 921.6 MHz, ref 38.4 MHz, SYN_SDIV = 8 (SPLL reference = 115.2 MHz)
SPLL = 4000 MHz, N= 34.72222, output divider 8 = 500 MHz
Icp = 2400 µA, ~200 kHz loop BW, output level +3.8 dBm

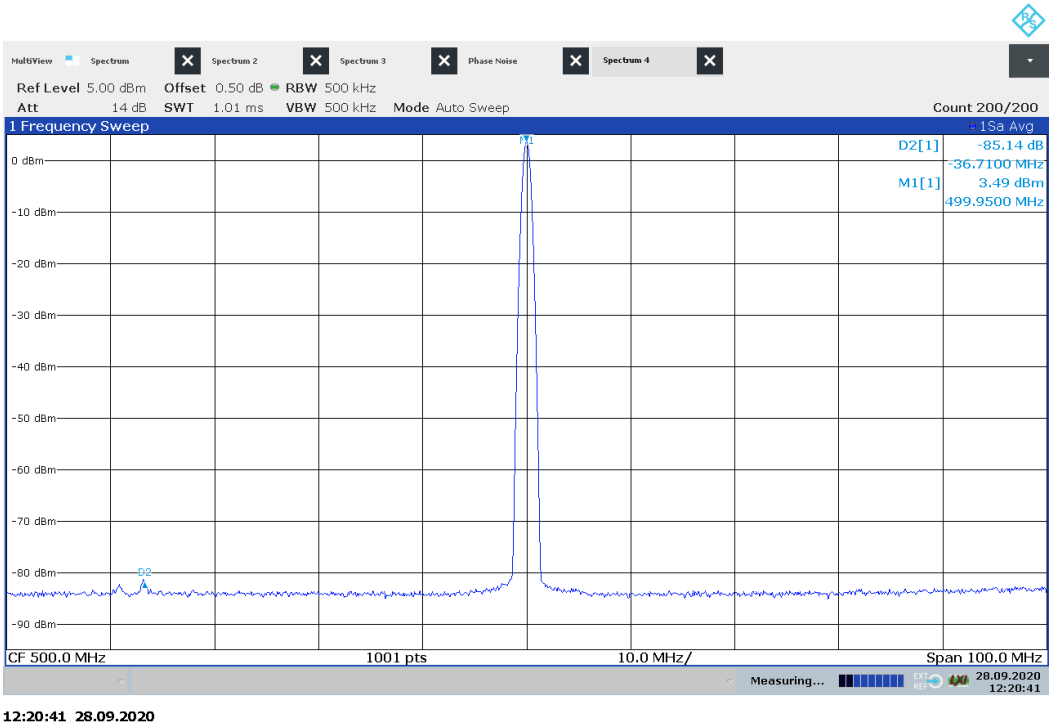


Figure 18 Spectral Plot at 500 MHz RF Output

Note: conditions for above plot:
REFPLL = 921.6 MHz, ref 38.4 MHz, SYN_SDIV = 8 (SPLL reference = 115.2 MHz)
SPLL = 4000 MHz, N= 34.72222, output divider 8 = 500 MHz
Icp = 2400 µA, ~200 kHz loop BW, output level +3.8 dBm

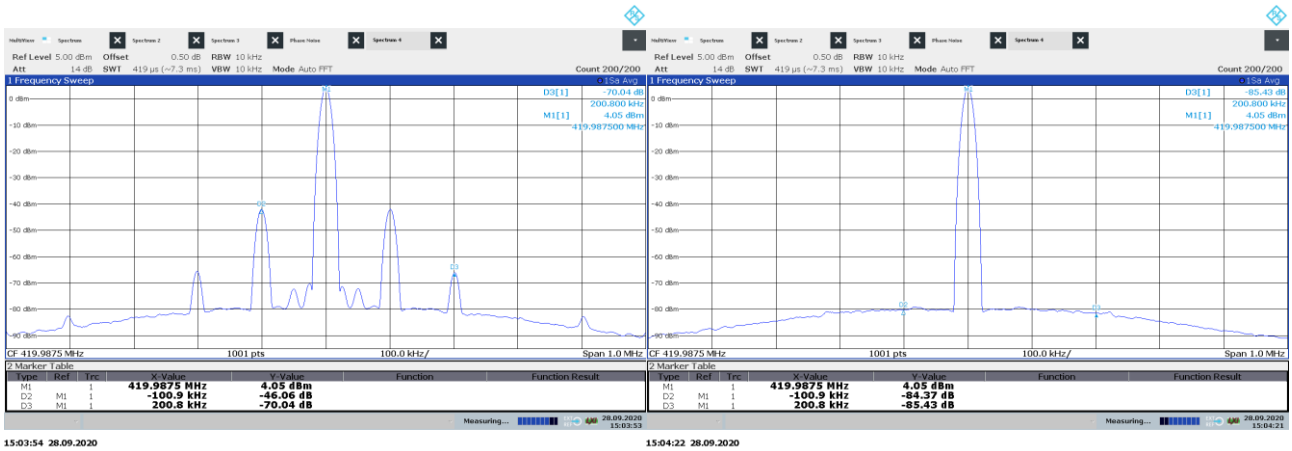
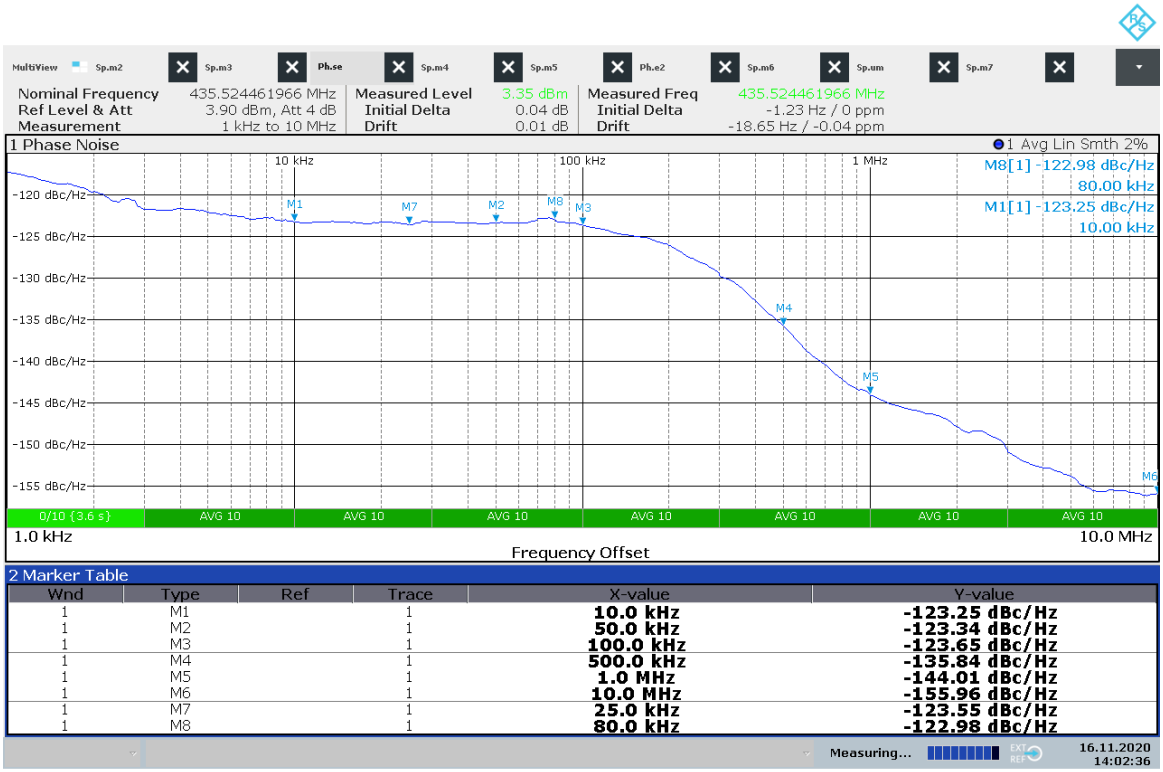


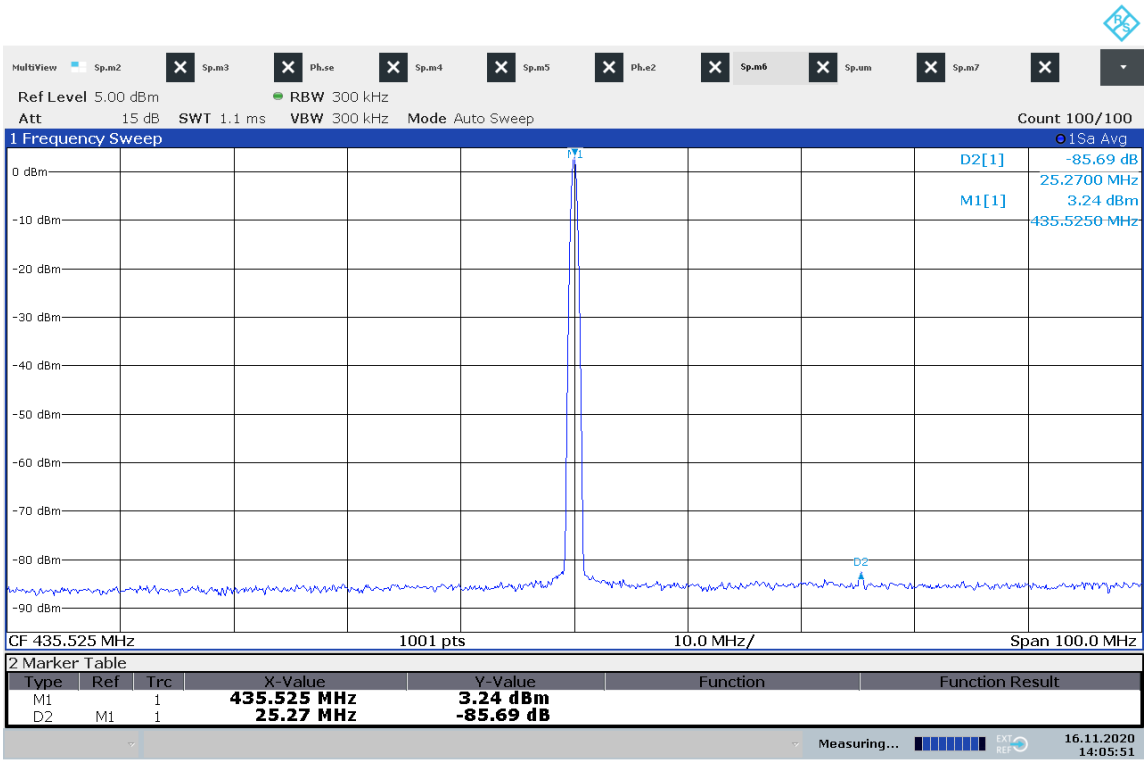
Figure 19 Spectral Plots at 419.9875 MHz RF Output showing spur avoidance

Note: conditions for above plot:
Left, REFPLL = 960 MHz, ref 38.4 MHz, SYN_SIDV = 8 (SPLL reference = 120 MHz), 100 kHz offset from the N=28 boundary, showing spurs. Right, REFPLL = 1036.8 MHz, ref 38.4 MHz, SYN_SIDV = 9 (SPLL reference = 115.2 MHz), N=29.1658.
SPLL = 3359.9 MHz, output divider 8 = 419.9875 MHz
Icp = 1600 µA, ~100 kHz loop BW, output level +3.8 dBm



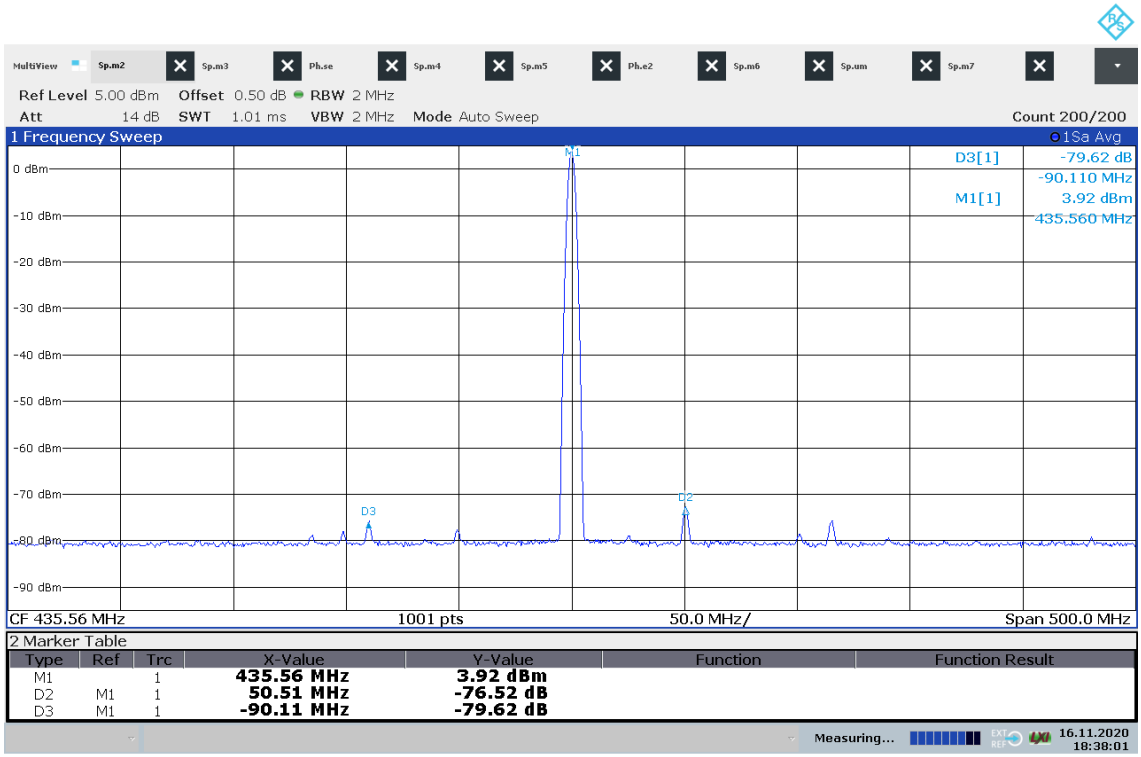
14:02:36 16.11.2020

Figure 20 Phase noise at 435.525 MHz RF Output



14:05:51 16.11.2020

Figure 21 Spectral Plot at 435.525 MHz RF Output, 100 MHz span.



18:38:02 16.11.2020

Figure 22 Spectral Plot at 435.525 MHz RF Output, 500 MHz span

7.5 Troubleshooting

The EV9400 is a complex RF system. If incorrectly programmed or modified, results will be at variance from datasheet performance. Please study the CMX940 datasheet along with this User Manual, associated schematics and layout drawings for the EV9400 board when troubleshooting. This section provides suggestions to help users resolve application issues that may be encountered.

7.5.1 RF SPLL Operation

Error Observed	Possible Cause	Remedy
PLL output unstable / noisy but on frequency	Unstable / low reference input level	Check the input reference connections and level. Check operation using the default on-board reference.
	Loop instability	The programmed PLL values may give a high gain peak. Check the loop components fitted and reprogram with a higher charge pump current or comparison frequency. Check for correct operation of the REF_PLL.
VCO unstable and on an unexpected frequency	Not calibrated.	Run calibration of the SVCO and check the returned values. Check continuity of the loop filter.
	Incorrect programming	Check that the expected REFPLL reference is provided. Check that the correct output division ratio (OUTPUT_DIV) has been selected.
High level spurious	Sub-optimal programming values	Avoid operating frequencies near integer or simple fraction boundaries: re-calculate the dividers for an alternative comparison frequency from different REF_PLL settings. Experiment with charge pump current and application of bleed current.
Low output level	Incorrect programming	Check that the correct LOOUT output port has been enabled and the output level set.

Table 8 RF SPLL – Possible Errors

7.5.2 REF PLL Operation

Error Observed	Possible Cause	Remedy
PLL output unstable / noisy but on frequency	Unstable / low reference input level	Check the input reference connections and level. Check operation using the default on-board reference.
VCO not close to programmed frequency	Not calibrated	Run calibration of the RVCO and check the returned values. Check that the appropriate value of inductor L6 is fitted for the wanted RVCO frequency of operation.
	Incorrect programming	Check that the correct division ratios have been selected

Table 9 REF PLL – Possible Errors

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the Evaluation Kit.

	Min.	Max.	Units
Supply (V_{IN} - V_{SS})	0	6.0	V
Current into or out of V_{IN} and V_{SS} pins	0	+0.5	A
Current into or out of any other connector pin	-20	+20	mA
Maximum Input Level		+10	dBm

8.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{IN} - V_{SS})		5.25	6.0	V

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
Reference (MCLK) Frequency = 38.4 MHz, V_{IN} = 5.5 V, T_{AMB} = +25°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{IN} (Regulators and reference on, CMX940 in reset)	1	–	6	–	mA
I_{IN} (CMX940 REF_PLL and VCO enabled, output buffers disabled)	1	–	14	–	mA
I_{IN} (CMX940 REF_PLL and SPLLs and VCOs enabled – cascaded system, divide by 4, -10 dBm output)	1	–	63	–	mA
I_{IN} (CMX940 REF_PLL and SPLLs and VCOs enabled – cascaded system, divide by 8, maximum output)	1	–	73	–	mA
SPLL / VCO Parameters					
Frequency Range		2720	–	4080	MHz
Divided Frequency Range at J5 / J7		48.571		2040	MHz
RF output level	2,3	-17	-10	+3	dBm
Output Impedance		–	50	–	Ω
Phase Noise (typical) at 25 kHz offset.	6	–	-123	–	dBc/Hz
Phase Noise (typical) at 1 MHz offset.		–	-141	–	dBc/Hz
Spurious Level	6	-	-76	-	dBc
REF_PLL / VCO Parameters					
Frequency Range	4	880	977	1075	MHz
RF output level	2, 3	–	-5 +4	–	dBm dBm
Output Impedance		–	50	–	Ω
Reference input (Ext Clk, J8)					
Input Impedance		–	High	–	Ω
Sensitivity	5	0.7	-	1.35	Vp-p
Microcontroller Interface					
For timings see CMX940 Datasheet					

Notes:

1. Total PCB current consumption, not current consumption of CMX940.
2. REF_LOOUT, divide by 1
3. REF_LOOUT, divide by 2 and higher.
4. Minimum calibration range using the default value of inductor L6 (4.7 nH, 2%).
5. Measured at J3, typically clipped sinewave.
6. Measured at 435.525 MHz output, cascaded system, REF_PLL at 921.6 MHz /8= 115.2 MHz SPLL reference. Spurious relative to maximum output and +/- 250 MHz offset from carrier.

ROHS Compliance

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