CMX90G702 6 - 18 GHz, +2 dB Positive Slope Gain Block RF Amplifier

Description

The CMX90G702 is a low-power 50 Ω gain block suitable for a wide variety of wireless applications operating in the 6 – 18 GHz frequency range.

The gain block has a positive gain-slope of +2 dB across the 6 – 16 GHz band, eliminating the need for equalisation and compensates for increasing system losses with frequency.

CMX90G702 is highly integrated for ease of use, minimising external component count and board area. RF ports are matched on-chip to 50 Ω with an output DC-blocking capacitor. An active bias circuit with enable function, allows the device to operate over a wide supply voltage of 2 to 5V with typical current of 22 mA.

The device is fabricated using a GaAs pHEMT process to provide a combination of high linearity, low noise and low DC power consumption.

An alternative part, CMX90G701, is available for applications that require less gain-slope compensation.

3x3mm VQFN-16 Package

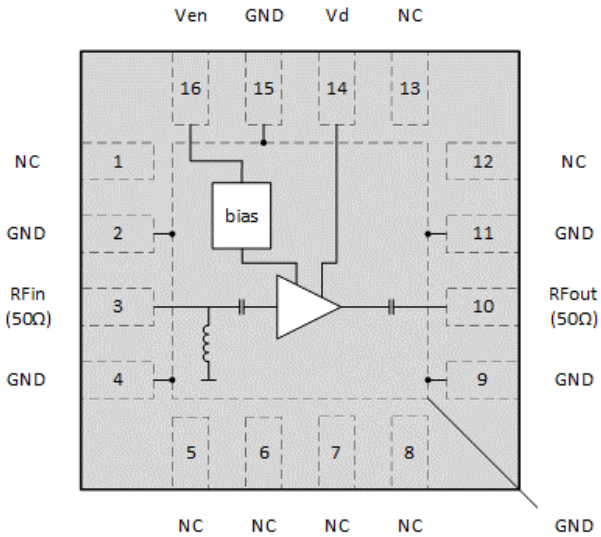
Product Features

- Wide frequency range 6 – 18 GHz
- Positive gain-slope +2 dB (6 – 16 GHz)
- Small signal gain 9.1 – 11.1 dB
- Single positive DC supply 2 – 5 V
- Low current consumption (typ 22 mA)
- Low noise figure 3 dB
- Output P1dB +9.3 dBm @ 12 GHz
- 1.8 V logic compatible enable
- 105 °C operating temperature (Vd ≤ 3.3 V)

Applications

- Satcom Ku-band
- Fixed wireless access (FWA)
- 5G infrastructure & backhaul
- X-band (8 – 12GHz)
- PA Modules
- Eliminate passive equaliser

Block Diagram



Ordering Information

Part Number	Description
CMX90G702QF-R705	7” Reel with 500 pieces
CMX90G702QF-R710	7” Reel with 1,000 pieces
EV90G702	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+12 dBm
Device Voltage (Vd, Ven)	+5.5 V
Case Temperature (Tc)	-40 to +85 °C (Vd > 3.3V), -40 to +105 °C (Vd ≤ 3.3V)
Junction Temperature (Tjmax)	165 °C (Process MTTF = 10^6 hours)
Storage Temperature	-40 to +125 °C
ESD Sensitivity	HBM 250 V (Class 1A), CDM 750 V (Class C2b)
MSL Level	Level 3

Exceeding the maximum ratings may result in damage or reduced device reliability.

Thermal Characteristics

Parameter	Rating
Thermal Resistance (Rjc)	540 °C/W (Tc = 85 °C, Vd = Ven = 5 V) 550 °C/W (Tc = 105 °C, Vd = Ven = 3.3 V)

Thermal resistance is junction-to-case, where case refers to the exposed die pad on the backside which is in contact with the board.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Frequency Range	6		18	GHz
Case Temperature (Tc) Vd > 3.3 V	-40		+85	°C
Case Temperature (Tc) Vd ≤ 3.3 V	-40		+105	°C
Device Voltage (Vd)	2		5	V
Enable Voltage (Ven)	0		5	V

The device will be tested under certain conditions, but performance is not guaranteed over the full range of recommended operating conditions.

ESD Caution

High-performance RF integrated circuits are highly sensitive to electrostatic discharge (ESD) and may contain unprotected inputs and outputs. Handling and assembly should be conducted in an ESD-controlled environment. It is recommended that ESD precautions and protocols are adopted to minimise the risk of electrostatic discharge and protect product integrity.

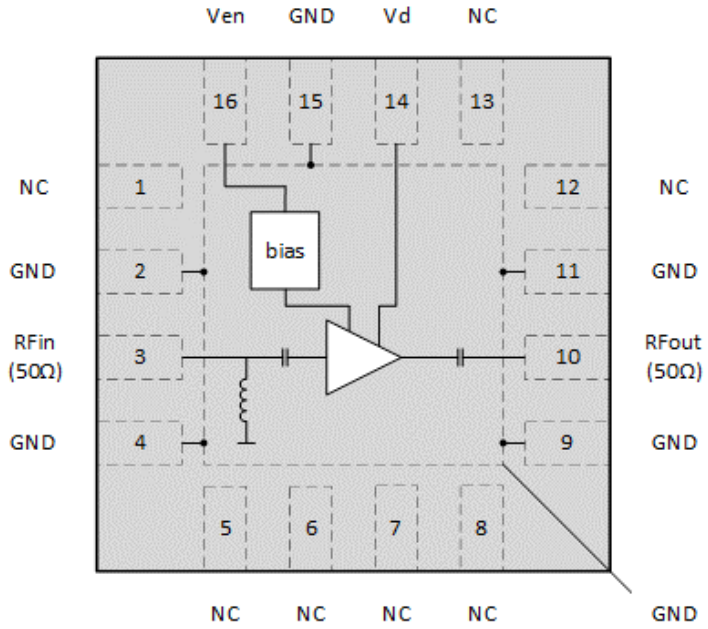
Electrical Specification

Results taken on EV90G702 EVB, where track losses have been de-embedded using the calibration line on the EV90G702 evaluation board.

Zo = 50 Ω, Vd = +5 V, Ven = +5 V, Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Frequency		6		18	GHz
Small Signal Gain	6 GHz		9.1		dB
Small Signal Gain	16 GHz		11.1		dB
Small Signal Gain	18 GHz		11.1		dB
Gain Slope	6 GHz to 16 GHz		+2		dB
Reverse Isolation	6 GHz to 18 GHz		>16		dB
P1dB	At 12 GHz		9.3		dBm
OIP3	Two-tone test Δf = 10 MHz, at 12 GHz, Pout/Tone = 0dBm	-	18.5	-	dBm
Noise Figure	12 GHz		2.8		dB
Input Return Loss	6 GHz to 18 GHz		>10		dB
Output Return Loss	6 GHz to 18 GHz		>10		dB
Device Current (Id)			22		mA
Ven (Logic 1 = Enabled)	Amplifier normal operation	1.8		5	V
Ven (Logic 0 = Standby)	Amplifier in standby mode	0		0.2	V
Id	Ven = 0 V		1.5		µA
Id	Ven = 0.2 V		15		µA
S21	Ven = 0 to 0.2 V		-11.6		dB
Ven Current (Ien)	Ven = 5 V		0.8		mA
Turn-On Time RFout: 10 % to 90 %	RFin = -10 dBm, 10 GHz		0.6		µs
Turn-Off Time RFout: 90 % to 10 %	RFin = -10 dBm, 10 GHz		0.9		µs

Pin Assignments



Top View

Pin	Name	Description
1	NC	Connect to GND
2	GND	Connect to GND
3	RFin	RF input. Internally matched to 50 Ω with DC path to ground to provide enhanced ESD robustness.
4	GND	Connect to GND
5	NC	Connect to GND
6	NC	Connect to GND
7	NC	Connect to GND
8	NC	Connect to GND
9	GND	Connect to GND
10	RFout	RF output. Internally matched to 50 Ω with integrated DC-blocking capacitor.
11	GND	Connect to GND
12	NC	Connect to GND
13	NC	Connect to GND
14	Vd	Voltage supply to amplifier
15	GND	Connect to GND
16	Ven	Amplifier enable input
Die pad	GND	DC and RF ground. Exposed die pad must be connected to GND.

Notes
CML recommends that all no connect (NC) pins are connected to ground.
The bottom exposed die pad must be connected to the ground plane on the board.

Typical Performance

The following plots show typical performance characteristics of CMX90G702 measured on the evaluation board (Part Number EV90G702). Board losses have been de-embedded from the measurement results using the through line that is included on the EV90G702.

RF typical performance Vd = Ven = 5.0 V, Ta = 25 °C, Z0 = 50 Ω

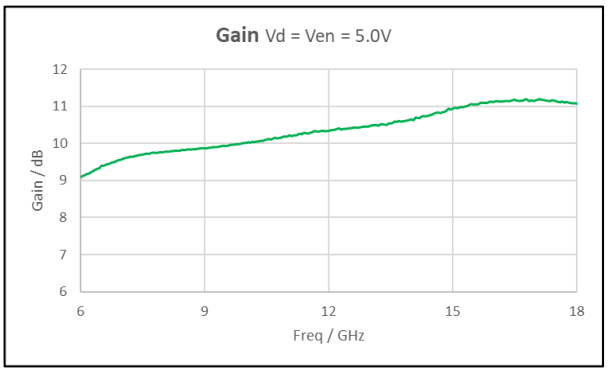


Figure 1: Gain Vd = Ven = 5.0 V

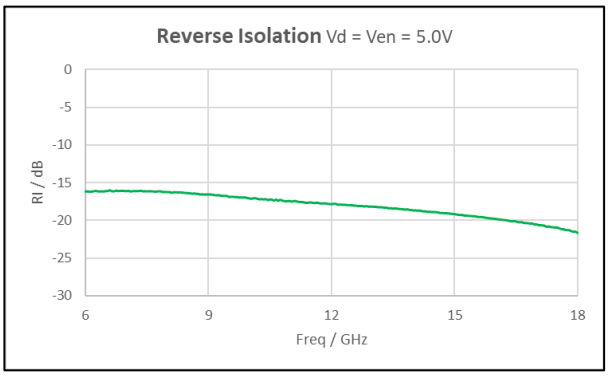


Figure 2: Reverse Isolation Vd = Ven = 5.0 V

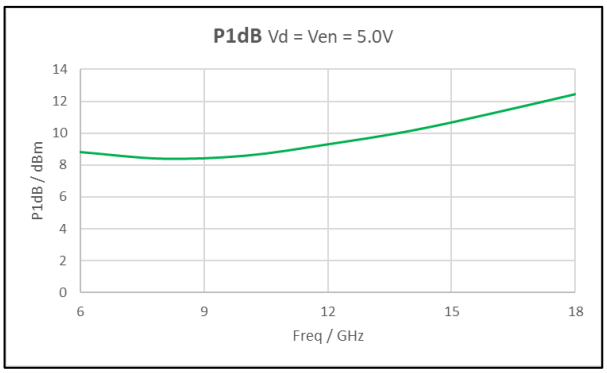


Figure 3: P1dB Vd = Ven = 5.0 V

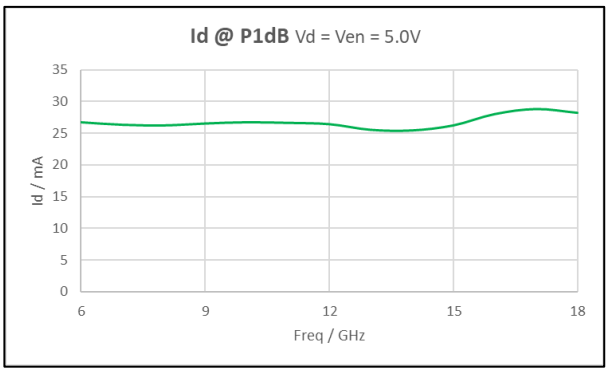


Figure 4: Id @ P1dB Vd = Ven = 5.0 V

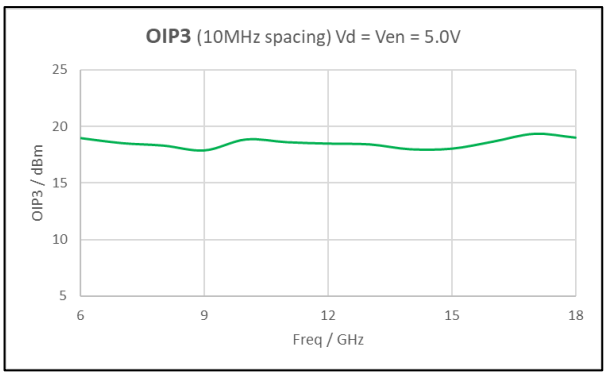


Figure 5: OIP3 (10MHz spacing) Vd = Ven = 5.0 V

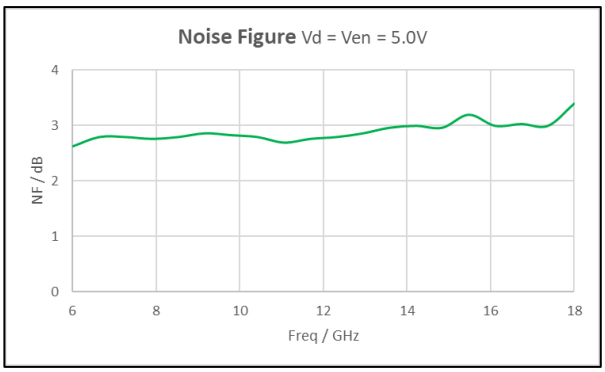


Figure 6: Noise Figure Vd = Ven = 5.0 V

RF typical performance Vd = Ven = 5.0 V, Ta = 25 °C, Z0 = 50 Ω (cont'd)

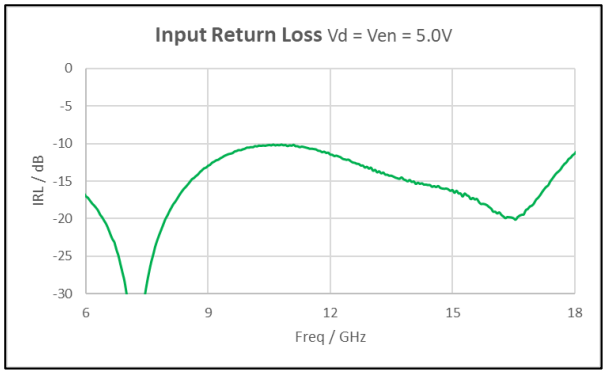


Figure 7: Input Return Loss Vd = Ven = 5.0 V

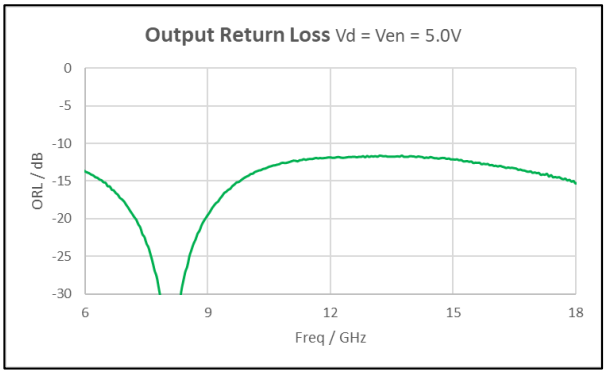


Figure 8: Output Return Loss Vd = Ven = 5.0 V

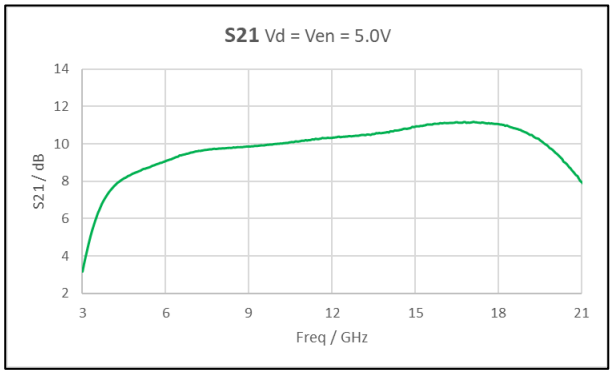


Figure 9: S21 Vd = Ven = 5.0 V

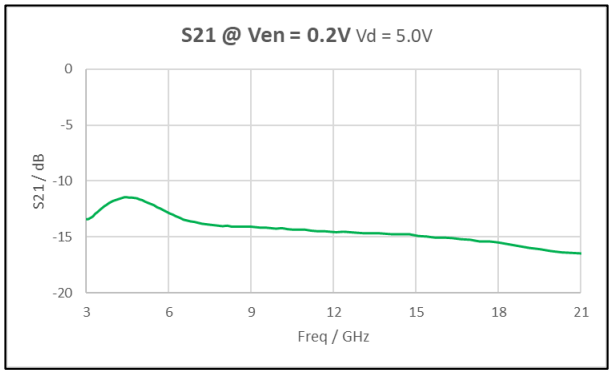


Figure 10: S21 @ Ven = 0.2 V Vd = 5.0 V

DC typical performance Vd = 5.0V, Ta = 25 °C

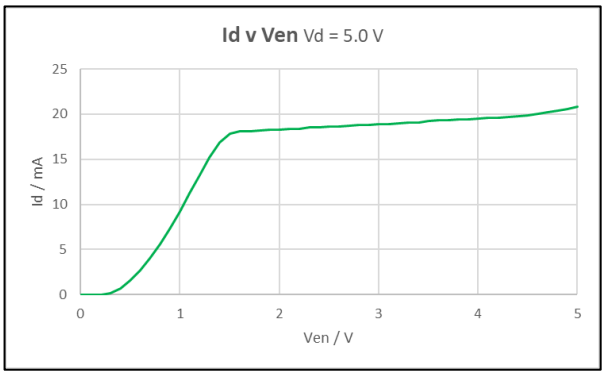


Figure 11: Id v Ven Vd = 5.0 V

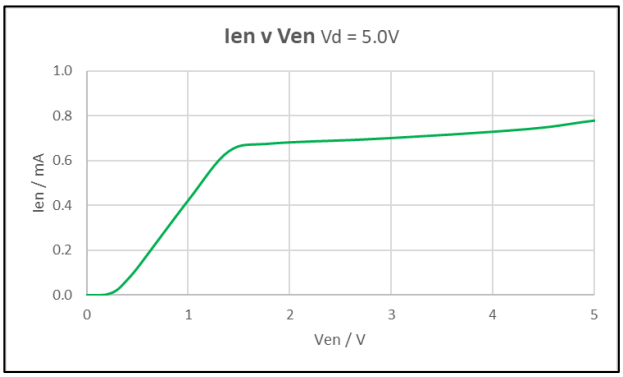


Figure 12: Ien v Ven Vd = 5.0 V

DC performance over voltage Ta = 25 °C

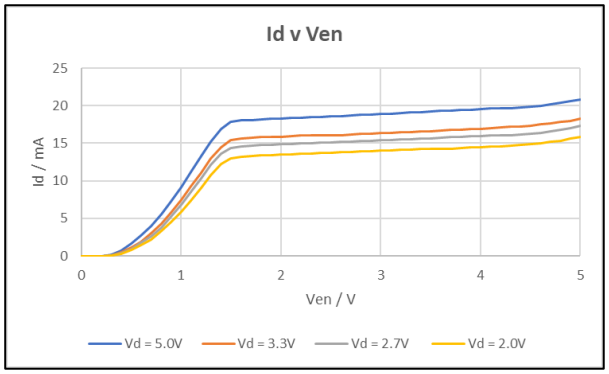


Figure 13: Id v Ven

RF performance over voltage Vd = Ven, Ta = 25 °C, Z0 = 50 Ω

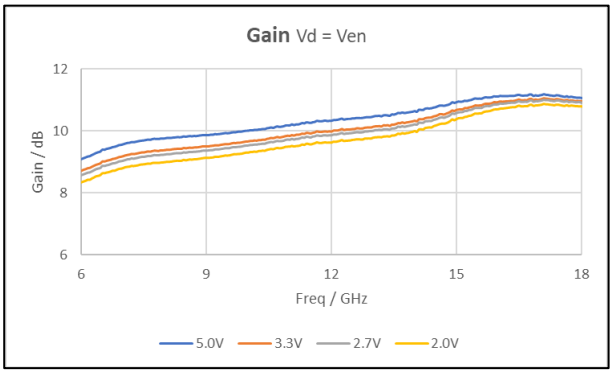


Figure 14: Gain Vd = Ven

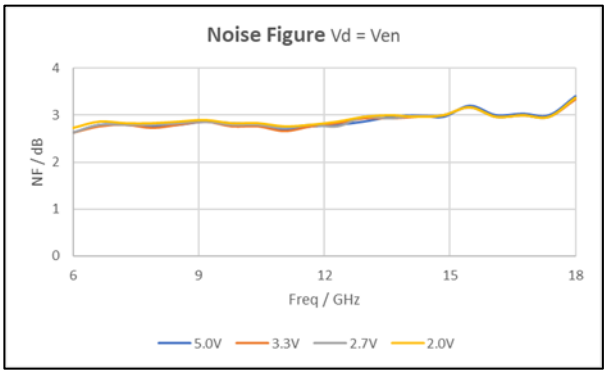


Figure 15: Noise Figure Vd = Ven

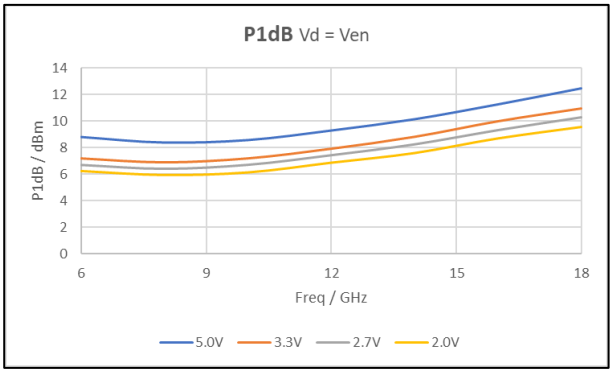


Figure 16: P1dB Vd = Ven

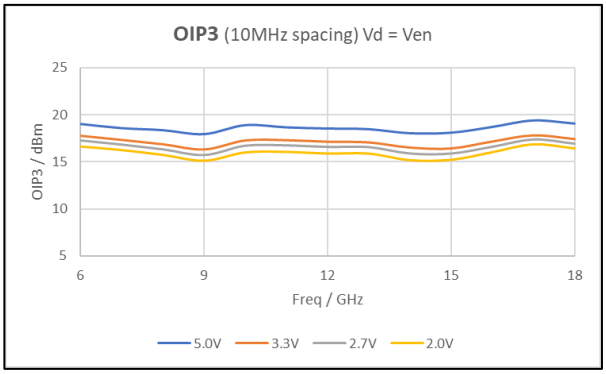


Figure 17: OIP3 (10 MHz spacing) Vd = Ven

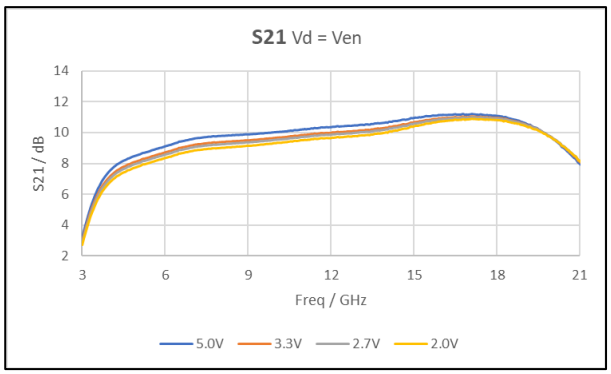


Figure 18: S21 Vd = Ven

RF over temperature

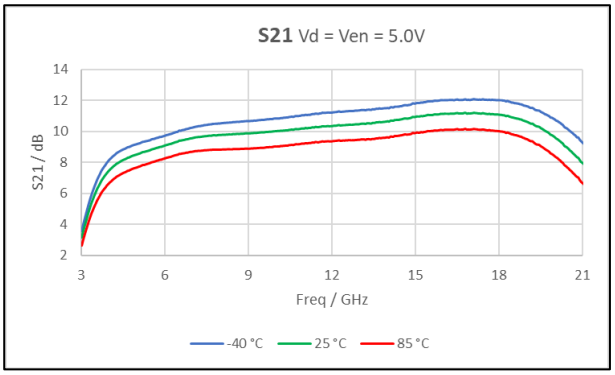


Figure 19: S21 Vd = Ven = 5.0 V

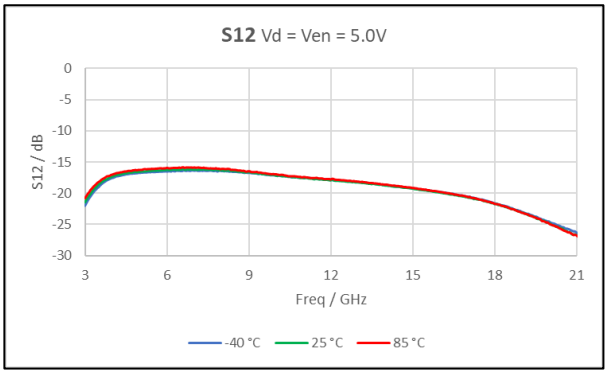


Figure 20: S12 Vd = Ven = 5.0 V

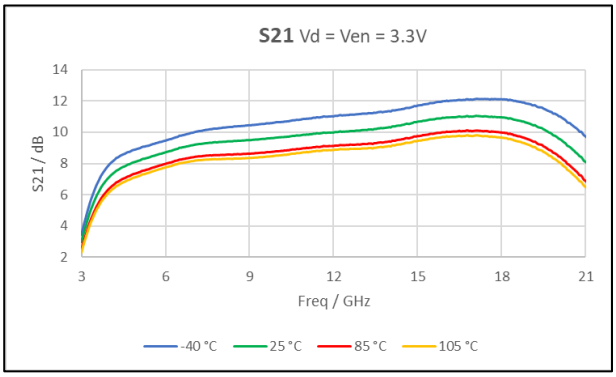


Figure 21: S21 Vd = Ven = 3.3 V

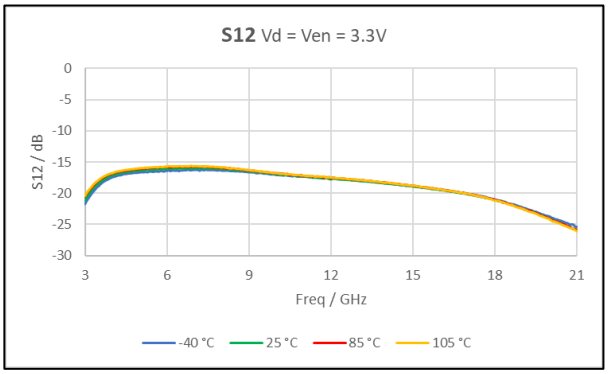


Figure 22: S12 Vd = Ven = 3.3 V

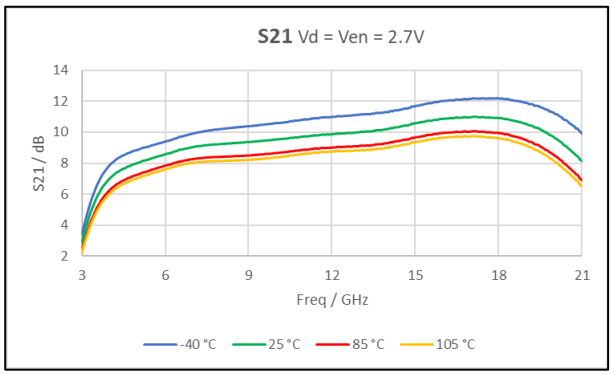


Figure 23: S21 Vd = Ven = 2.7 V

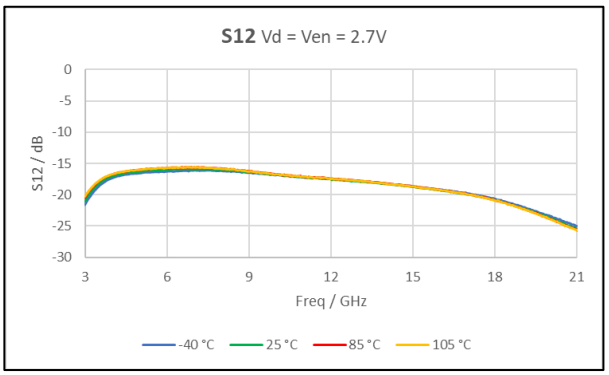


Figure 24: S12 Vd = Ven = 2.7 V

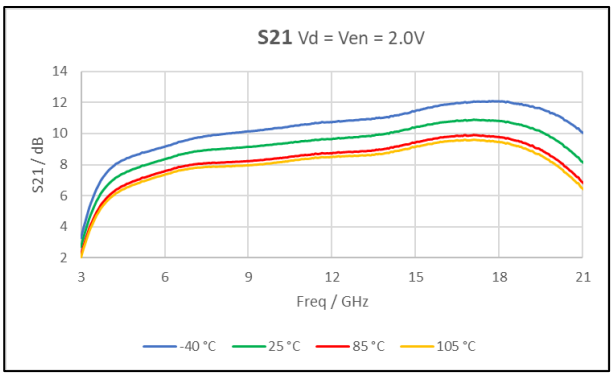


Figure 25: S21 Vd = Ven = 2.0 V

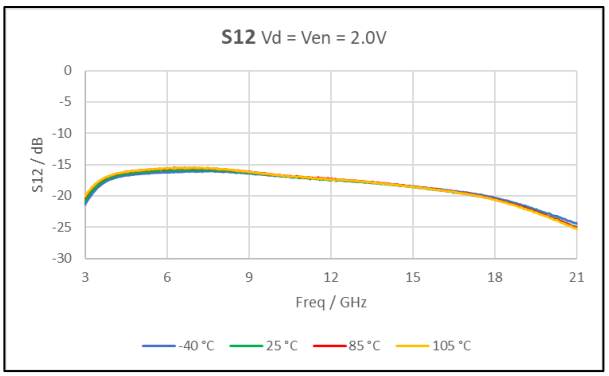


Figure 26: S12 Vd = Ven = 2.0 V

RF performance over temperature Vd = Ven, Z0 = 50 Ω

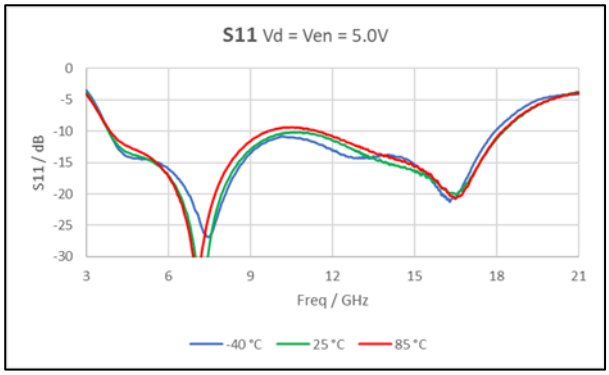


Figure 27: S11 Vd = Ven = 5.0 V

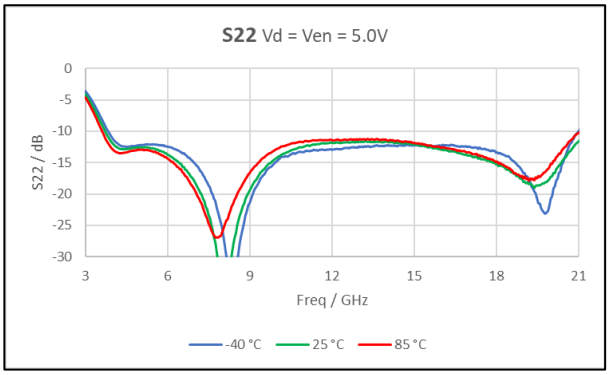


Figure 28: S22 Vd = Ven = 5.0 V

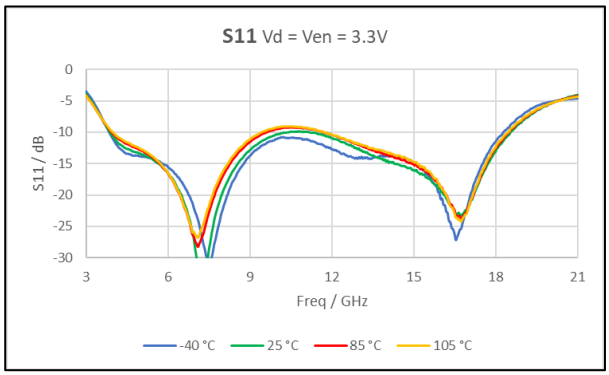


Figure 29: S11 Vd = Ven = 3.3 V

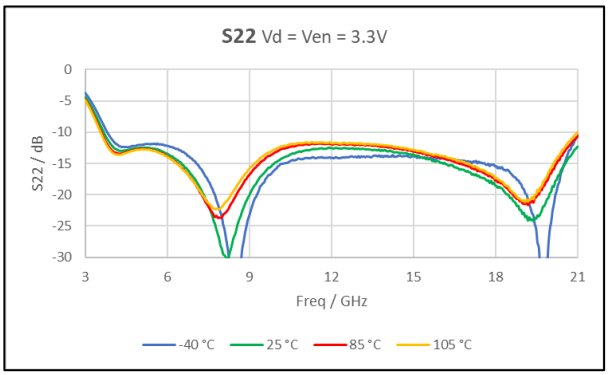


Figure 30: S22 Vd = Ven = 3.3 V

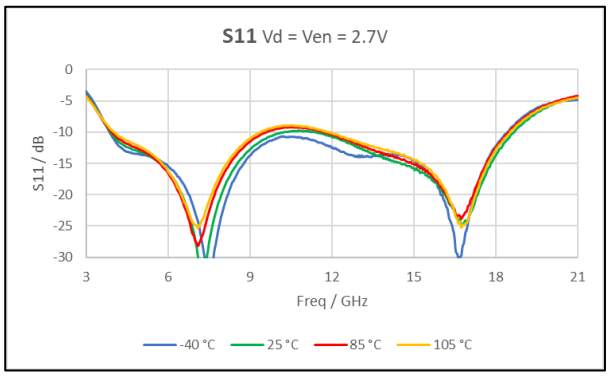


Figure 31: S11 Vd = Ven = 2.7 V

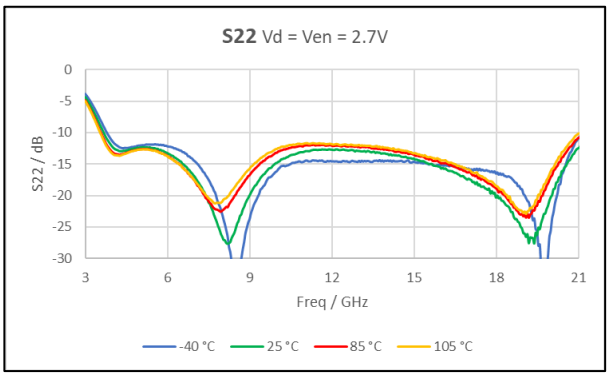


Figure 32: S22 Vd = Ven = 2.7 V

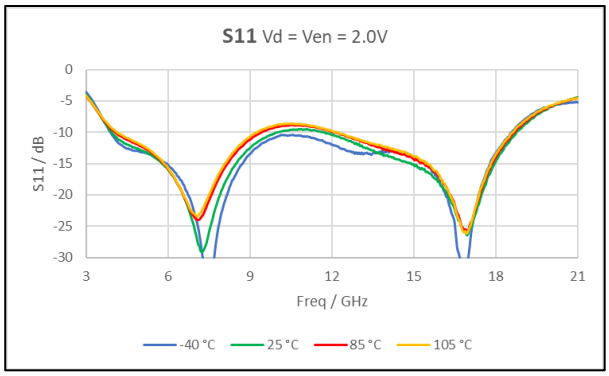


Figure 33: S11 Vd = Ven = 2.0 V

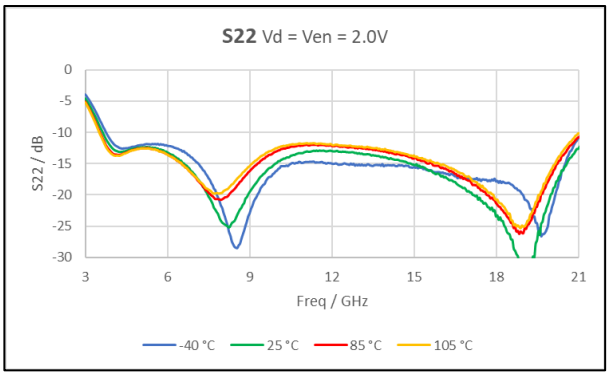


Figure 34: S22 Vd = Ven = 2.0 V

RF performance over temperature Vd = Ven, Z0 = 50 Ω

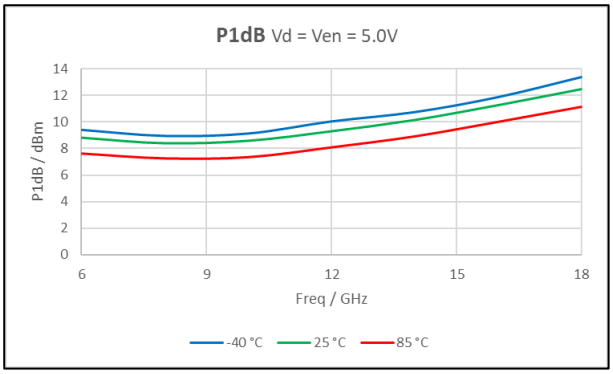


Figure 35: P1dB Vd = Ven = 5.0 V

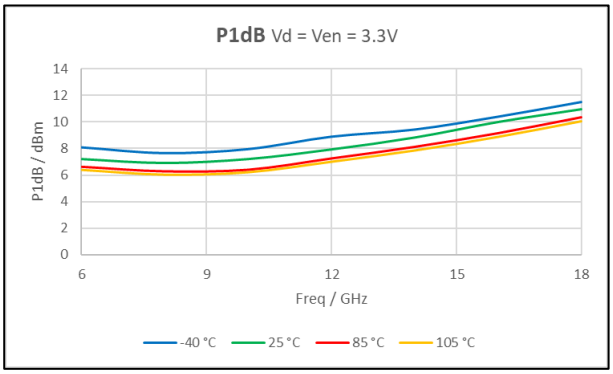


Figure 36: P1dB Vd = Ven = 3.3 V

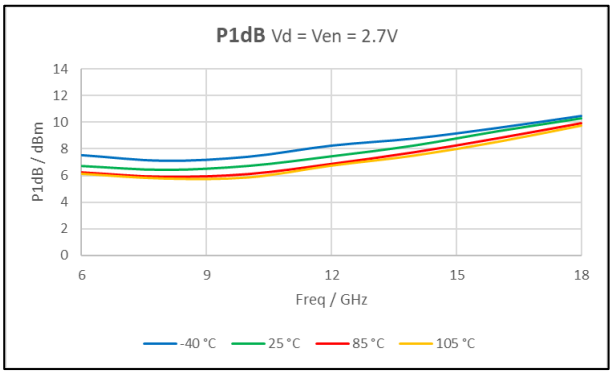


Figure 37: P1dB Vd = Ven = 2.7 V

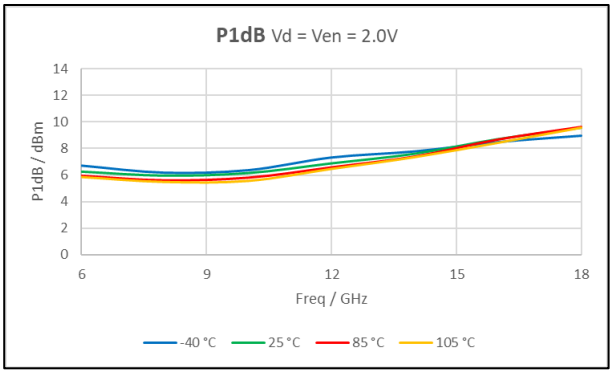


Figure 38: P1dB Vd = Ven = 2.0 V

DC performance over temperature

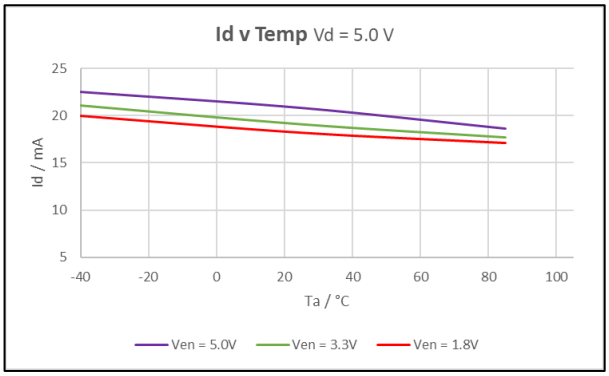


Figure 39: Id v temp Vd = 5.0 V

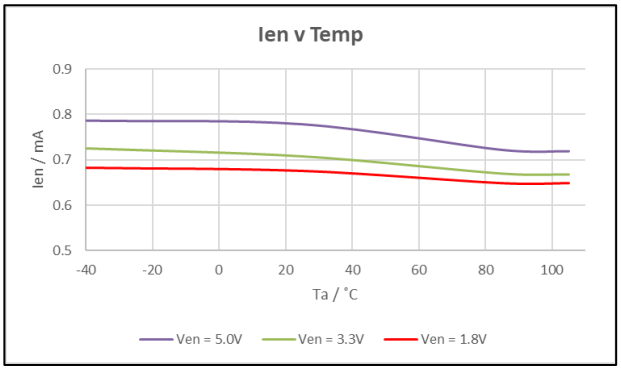


Figure 40: Ien v temp

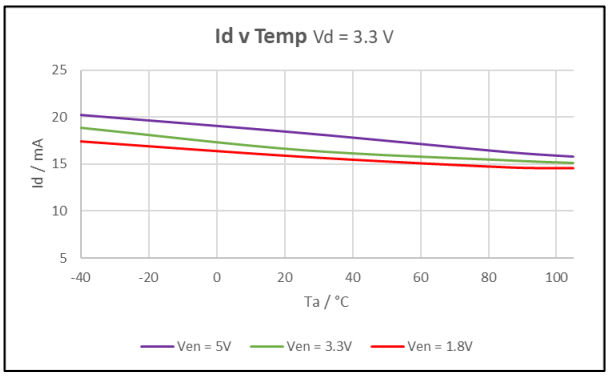


Figure 41: Id v temp Vd = 3.3 V

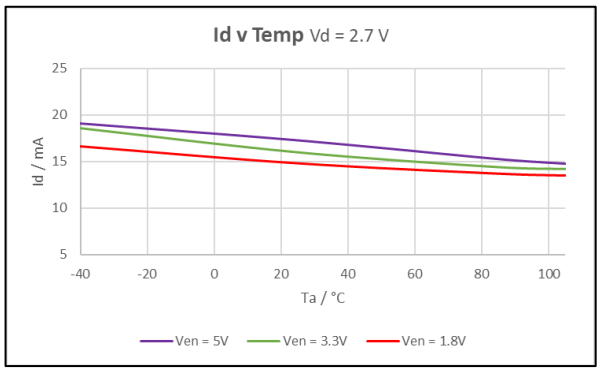


Figure 42: Id v temp Vd = 2.7 V

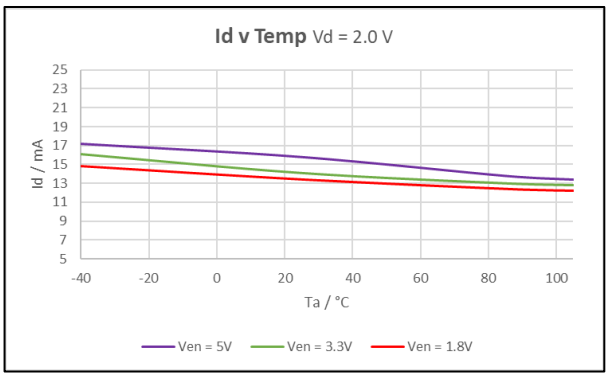


Figure 43: Id v temp Vd = 2.0 V

Application Information

Schematic Diagram

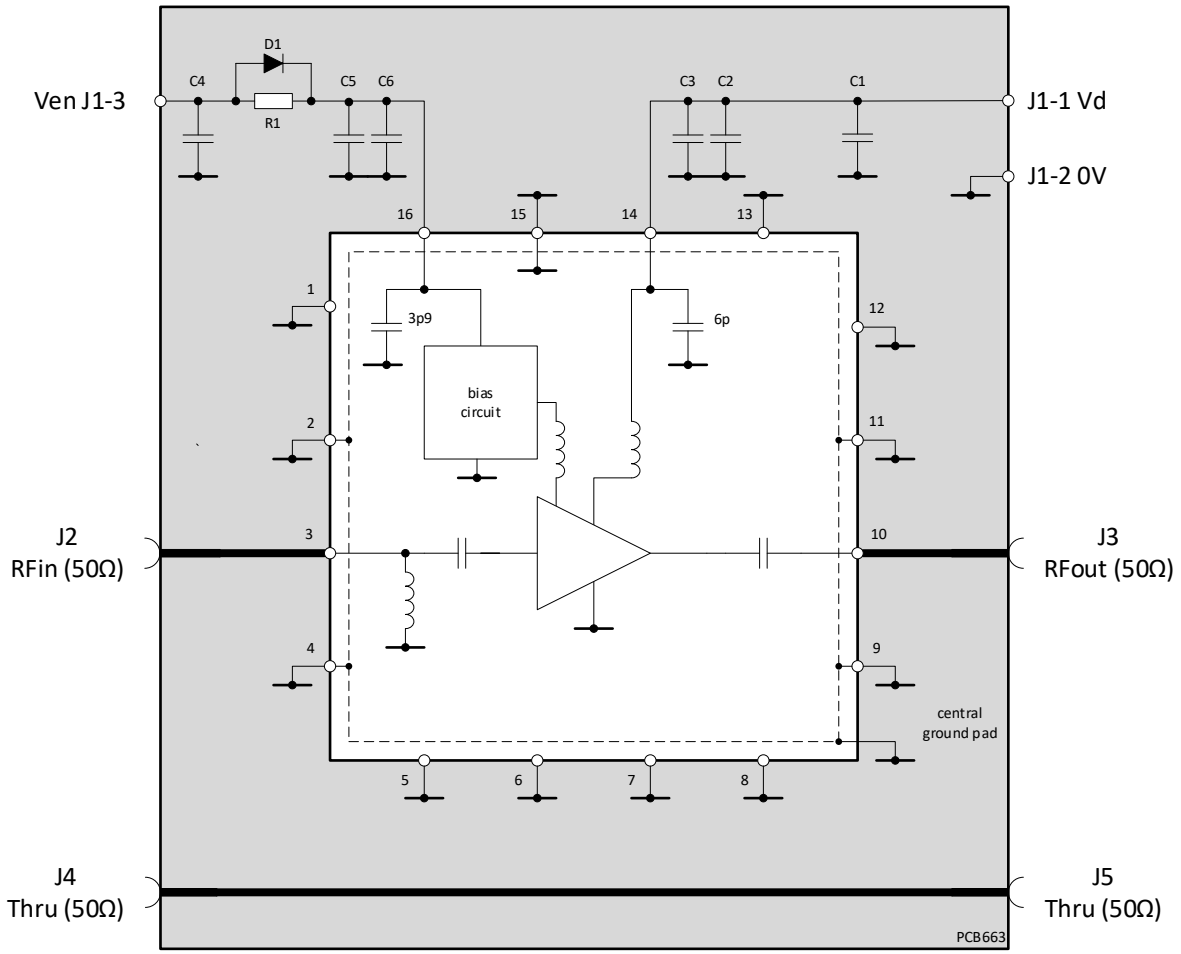


Figure 44: EV90G702 Schematic

Bill Of Materials (BOM)

Reference Designator	Value	Size	Description
C1	1 µF	0603	16 V, ±10 %
C2	10 nF	0402	16 V, ±10 %
C3	DNF	0402	
C4	10 nF	0402	16 V, ±10 %
C5	1 nF	0402	25 V, ±5 %
C6	DNF	0402	
R1	0 Ω	0402	0.063 W
D1	DNF	SOD-523F	

Notes

- DNF = Do not fit component

PCB Layout

Careful layout of the printed circuit board (PCB) is essential for optimum RF and thermal performance. The recommended layout, including ground via pattern underneath the device, may be taken from the evaluation board (Part Number EV90G702).

The PCB consists of a top layer of MT40 backed by 2 layers of FR-4 with a total thickness of 1.632 mm (Figure 45) and the EV90G702 PCB (Figure 46) is 20 mm x 45 mm. The coplanar RF transmission lines have a width of 0.33 mm with a

gap of 0.14 mm to ground either side. The through line length has been reduced by 3mm to account for the length of the device.

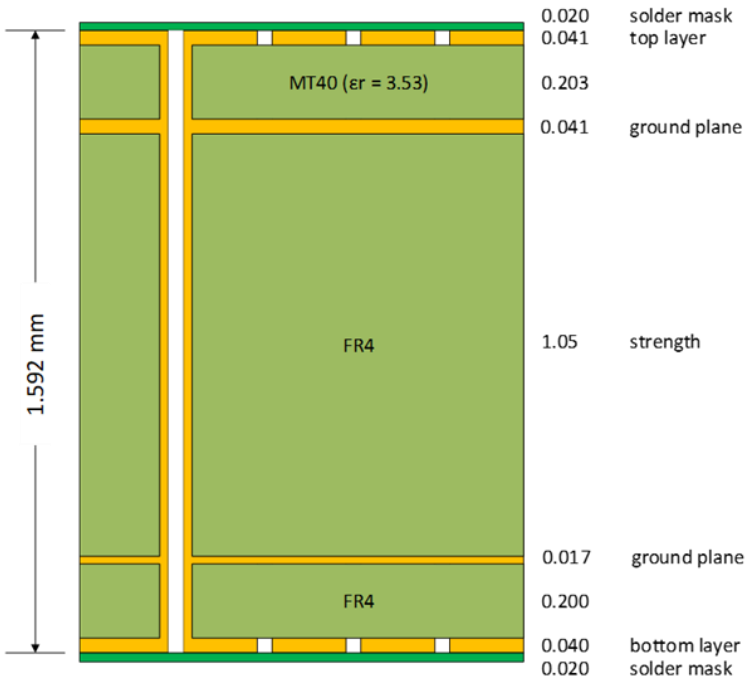


Figure 45: EV90G702 Layer Stack

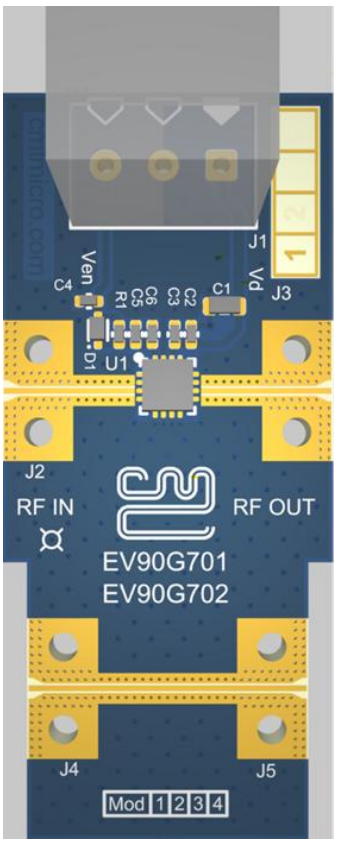


Figure 46: EV90G702 PCB Top Layer View

Thermal Design

The primary RF/DC ground and thermal path is via the exposed die pad on the backside of the package, which must be connected to the PCB ground plane. An array of plated through-hole vias directly underneath the die pad area is essential to conduct heat away and minimise ground inductance. A typical solution will have 9 grounding vias connecting

the top layer to the bottom layer, with inner diameter of 0.2 mm (and 0.025 mm plating) on a 0.55 mm grid pattern. The vias do not need to be filled. The PCB layout should provide a thermal radiator appropriate for the intended operation, adding as much copper to inner and outer layers as possible to avoid excessive junction temperature.

Device junction temperature (Tj) can be calculated using Tj = Tc + (Pdiss x Rjc) where Pdiss = Pdc + Pin – Pout and Tc is the case temperature on the backside of the package (die pad) in contact with the PCB.

Ven Input

The device is enabled by applying a voltage between 1.8 V and 5.0 V to pin 16 (Ven). The resulting Id taken by the device is relatively independent of the Ven voltage applied. If the enable feature is not required, the Ven pin can be connected to the same voltage as Vd.

The device can be placed into standby mode when not in use by setting Ven low (<0.2V) to disable all circuitry.

If lower Ien and Id leakage current and/or if the highest forward isolation is needed in standby mode, a diode can be used in series with the Ven pin to increase the switch-on threshold of the device. This can be particularly important at elevated temperatures. Some suggested diodes in suitable packages (SOD-523F) for the evaluation board are:

- 1N914BWT-D PN fast switching diode
- BAT43XV2-D Schottky diode

Evaluation Board & Bias Procedure

In general, sequencing of the Vd and Ven supplies is not necessary however applying Vd before or simultaneously with Ven is recommended.

The separate through line can be used to measure the evaluation board and connector losses. These results can then be used to de-embed the device performance from evaluation board measurements.

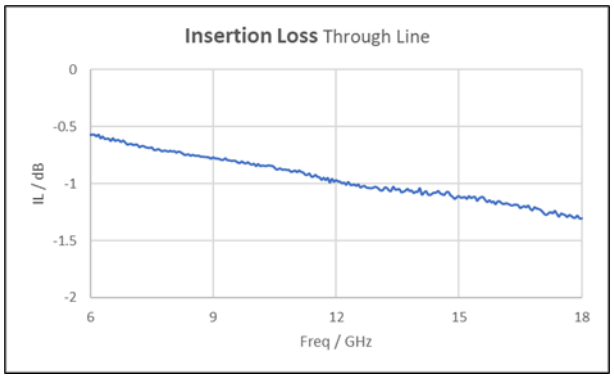


Figure 47: Insertion Loss – through line

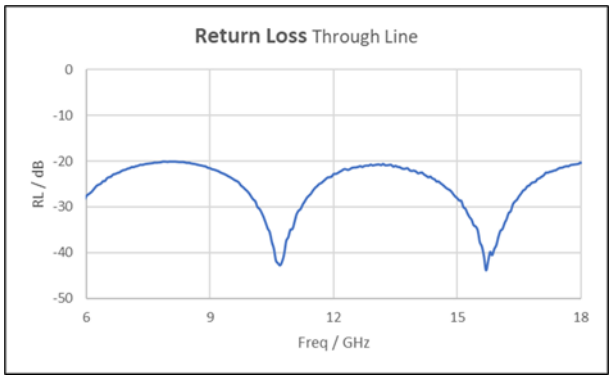
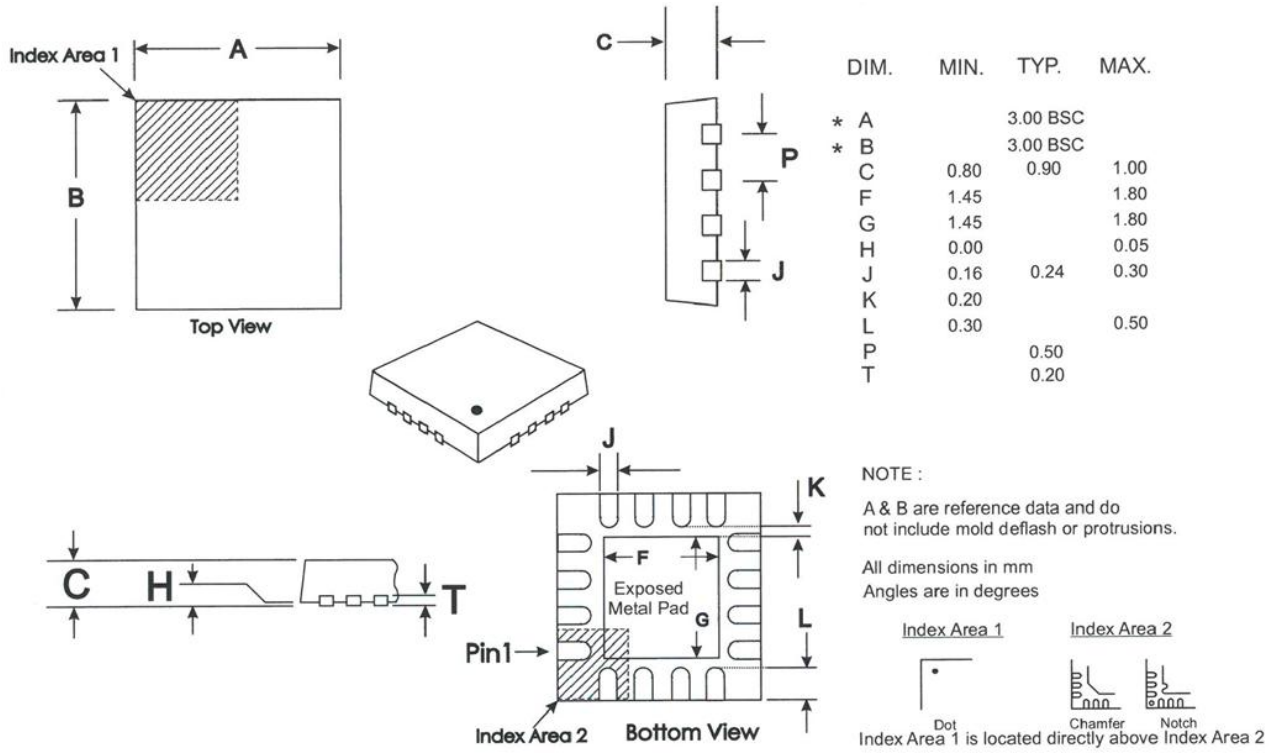


Figure 48: Return Loss – through line

Package Outline

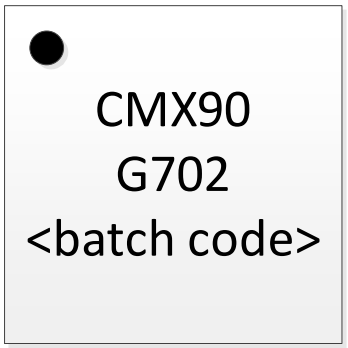
16-lead 3 x 3 mm VQFN Package (QF)



DIM.	MIN.	TYP.	MAX.
* A		3.00 BSC	
* B		3.00 BSC	
C	0.80	0.90	1.00
F	1.45		1.80
G	1.45		1.80
H	0.00		0.05
J	0.16	0.24	0.30
K	0.20		
L	0.30		0.50
P		0.50	
T		0.20	

Package Marking

Pin 1 indicator (dot) and 3 rows of text for device identification.



Line 1: CMX90 SµRF series

Line 2: 4-character part code

Line 3: Batch code

Revision History

Issue	Description	Date
2	Minor editorial changes	April 2023
1	First release – product launch	November 2022

ROHS Compliance

CML Micro certifies, to the best of our knowledge, that its products comply with **RoHS directive (2011/65/EU)**, as amended by **Directive (EU) 2015/863.**

REACH Compliance

CML Micro certifies, to the best of our knowledge, that its products do not contain any of the banned substances specified in the SVHC list at https://echa.europa.eu/candidate-list-table. CML Micro are committed to ensuring the safety of products and the compliance with regulations. Publications will be updated in the event that REACH control is compromised.

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