

CMX90B702 Low Current/Noise Gain Block 23 – 29.5 GHz

Description

The CMX90B702 is a low-current 50 Ω gain block suitable for a wide variety of wireless applications covering 23 – 29.5 GHz.

CMX90B702 is highly integrated to minimize external component count and board area. RF ports are matched on-chip to 50 Ω with an output DC-blocking capacitor. An active bias circuit helps maintain performance over a wide temperature range and supply voltage of 3 – 5 V.

The device is an easy-to-use gain block with fast enable circuit and dual-bias mode for system optimization, selecting bias of 10 mA or 15 mA.

CMX90B702 is fabricated using a GaAs pHEMT process to provide optimum gain, linearity, and noise together with low DC power consumption.

A footprint-compatible variant, CMX90B701, is available for applications covering 17 – 23 GHz.

Applications

- 5G mmWave Infrastructure
- Satcom (K and Ka band)
- Microwave Backhaul
- Fixed Wireless Access (FWA)
- 24 GHz ISM band

Ordering Information

Part Number	Description
CMX90B702QF-R705	7" Reel with 500 pieces
CMX90B702QF-R710	7" Reel with 1,000 pieces
EV90B702	Evaluation board

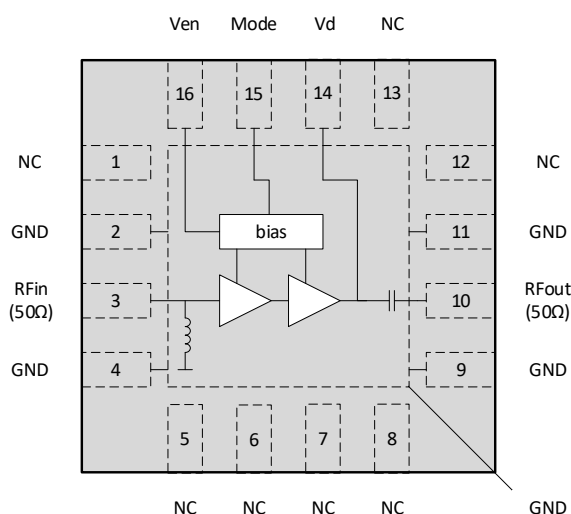


3x3mm VQFN-16 Package

Product Features

- Frequency range 23 – 29.5 GHz
- Small signal gain 17.5 dB
- Single positive DC supply 3 – 5 V
- Low power consumption 40 mW
- Output P1dB +5 dBm @ 26 GHz
- Output IP3 +15 dBm @ 26 GHz
- Noise figure 4 dB
- Dual-bias mode (low/high setting)
- 105 °C operating temperature

Block Diagram



Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+6 dBm
Device Voltage (Vd, Ven)	+5.5 V
Case Temperature (Tc)	-40 to +85 °C (Vd ≤ 5 V, high or low mode) -40 to +105 °C (Vd ≤ 4V, high mode) -40 to +105 °C (Vd ≤ 5V, low mode)
Junction Temperature (Tjmax)	165 °C (Process MTTF = 10 ⁷ hours)
Storage Temperature	-40 to +125 °C
ESD Sensitivity	HBM 250 V (Class 1A), CDM 500 V (Class C2a)
MSL Level	Level 3

Exceeding the maximum ratings may result in damage or reduced device reliability.

Thermal Characteristics

Parameter	Rating
Thermal Resistance (Rjc)	719 °C/W (Tc = 85 °C) 753 °C/W (Tc = 105 °C)

Thermal resistance is junction-to-case, where case refers to the exposed die pad on the backside which is in contact with the board.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Frequency Range	23		29.5	GHz
Case Temperature (Tc) Vd ≤ 5 V, high or low mode	-40		+85	°C
Case Temperature (Tc) Vd ≤ 4 V, high mode Vd ≤ 5 V, low mode	-40		+105	°C
Device Voltage (Vd)	3		5	V
Enable Voltage (Ven)	0		5	V

The device will be tested under certain conditions, but performance is not guaranteed over the full range of recommended operating conditions.

ESD Caution



High-performance RF integrated circuits are highly sensitive to electrostatic discharge (ESD) and may contain unprotected inputs and outputs. Handling and assembly should be conducted in an ESD-controlled environment. It is recommended that ESD precautions and protocols are adopted to minimise the risk of electrostatic discharge and protect product integrity.

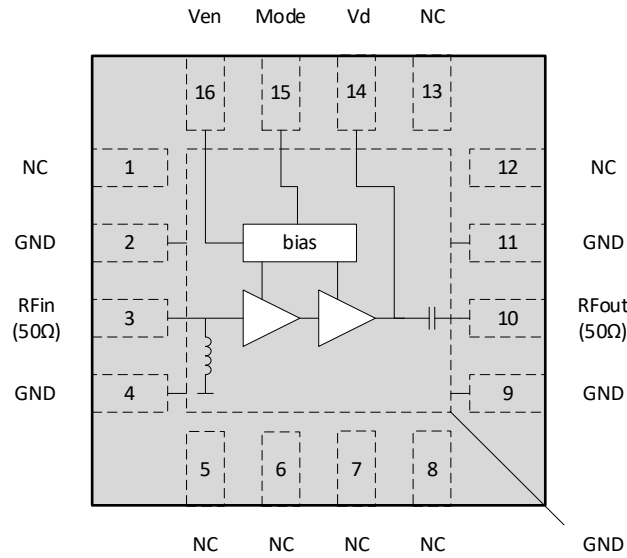
Electrical Specification

Results taken on EV90B702 EVB, where track losses have been de-embedded using the calibration line on the EV90B702 evaluation board.

$Z_0 = 50 \Omega$, $V_d = +4 \text{ V}$, $V_{en} = +4 \text{ V}$, $V_{mode} = \text{Low Current}$, $T_a = +25^\circ \text{C}$ (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Frequency		23		29.5	GHz
Small Signal Gain	23 GHz		17.5		dB
Small Signal Gain	26 GHz		17.5		dB
Small Signal Gain	29.5 GHz		17		dB
Gain Flatness	23 GHz to 29.53 GHz		± 1		dB
Reverse Isolation	23 GHz to 29.5 GHz		>30		dB
P1dB	At 26 GHz		5		dBm
OIP3	Two-tone test $\Delta f = 100 \text{ MHz}$, at 26 GHz, Pout/Tone = -7dBm	-	15	-	dBm
Noise Figure	26GHz		4		dB
Input Return Loss	23 GHz to 29.5 GHz		6		dB
Output Return Loss	23 GHz to 29.5 GHz		8		dB
Device Current (I_d)			10		mA
Ven (Logic 1 = Enabled)	Amplifier normal operation	1.8		5	V
Ven (Logic 0 = Standby)	Amplifier in standby mode	0		0.2	V
I_d	$V_d = 5 \text{ V}$, $V_{en} = 0 \text{ V}$		1.5		μA
S21	$V_{en} = 0$ to 0.2 V		<-20		dB
Ven Current (I_{en})	$V_{en} = 4 \text{ V}$		0.37		mA
Turn-On Time RFout: 10 % to 90 %	$R_{Fin} = -10 \text{ dBm}$, 26 GHz		0.6		μs
Turn-Off Time RFout: 90 % to 10 %	$R_{Fin} = -10 \text{ dBm}$, 26 GHz		0.9		μs

Pin Assignments



Pin	Name	Description
1	NC	Connect to GND
2	GND	Connect to GND
3	RFin	RF input. Internally matched to 50 Ω with DC path to ground to provide enhanced ESD robustness.
4	GND	Connect to GND
5	NC	Connect to GND
6	NC	Connect to GND
7	NC	Connect to GND
8	NC	Connect to GND
9	GND	Connect to GND
10	RFout	RF output. Internally matched to 50 Ω with integrated DC-blocking capacitor.
11	GND	Connect to GND
12	NC	Connect to GND
13	NC	Connect to GND
14	Vd	Voltage supply to amplifier
15	Mode	Mode pin to select current mode – GND = Low Current and O/C = High Current
16	Ven	Amplifier enable input
Die pad	GND	DC and RF ground. Exposed die pad must be connected to GND.

Notes

CML recommends that all no connect (NC) pins are connected to ground.

The bottom exposed die pad must be connected to the ground plane on the board.

Typical Performance

The following plots show typical performance characteristics of CMX90B702 measured on the evaluation board (Part Number EV90B702). Board losses have been de-embedded from the measurement results using the through line included on the EV90B702.

RF typical performance: $V_d = V_{en} = 4.0\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$, $Z_0 = 50\text{ }\Omega$

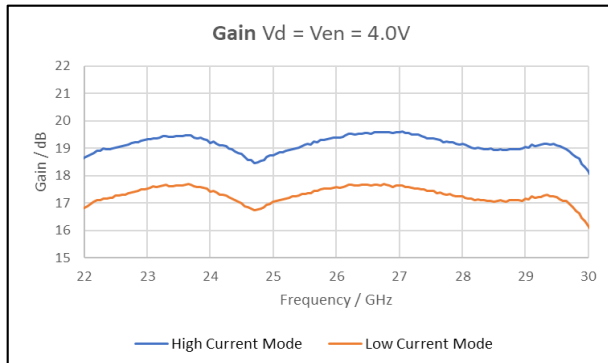


Figure 1: Gain $V_d = V_{en} = 4.0\text{ V}$

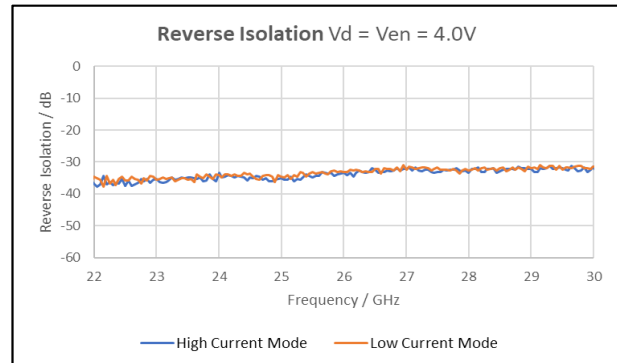


Figure 2: Reverse Isolation $V_d = V_{en} = 4.0\text{ V}$

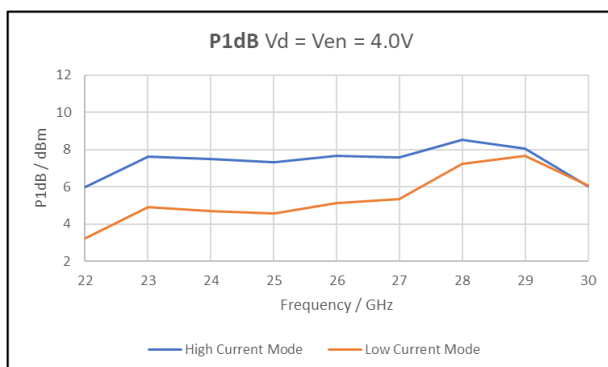


Figure 3: P1dB $V_d = V_{en} = 4.0\text{ V}$

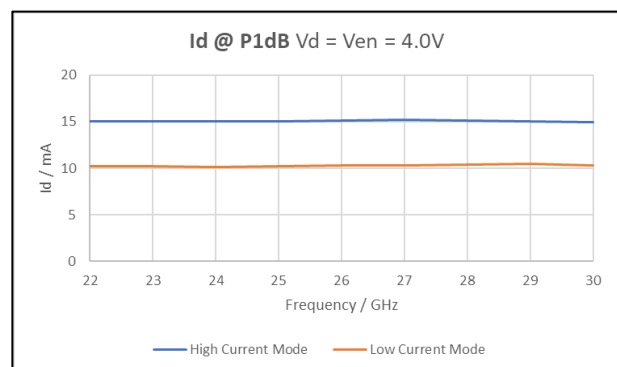


Figure 4: Id @ P1dB $V_d = V_{en} = 4.0\text{ V}$

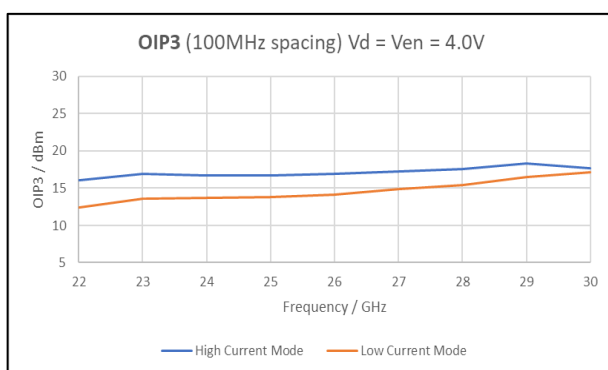


Figure 5: OIP3 100 MHz spacing, $P_{out} = -7\text{ dBm/ton}$, $V_d = V_{en} = 4.0\text{ V}$

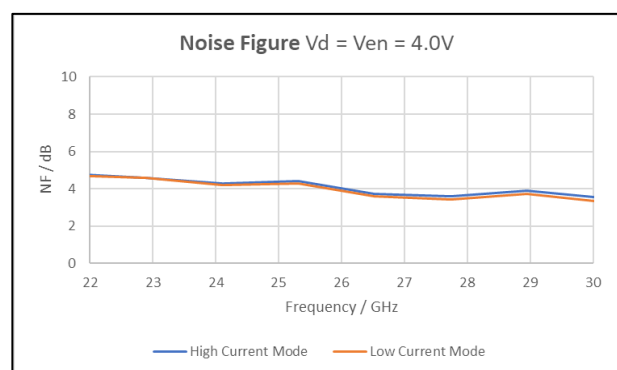
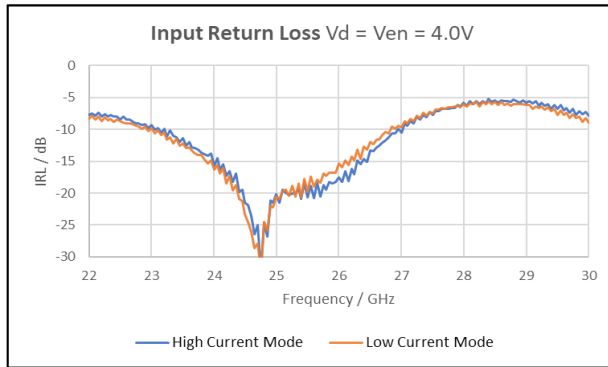
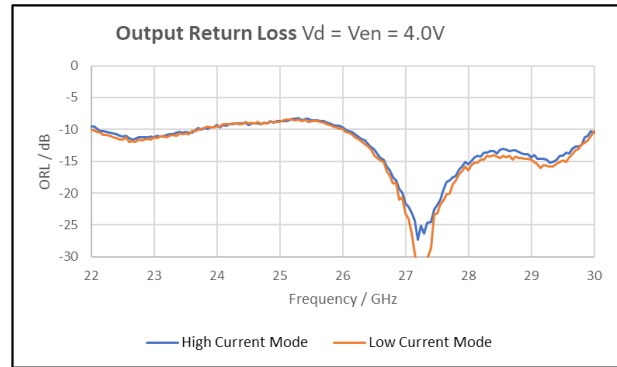
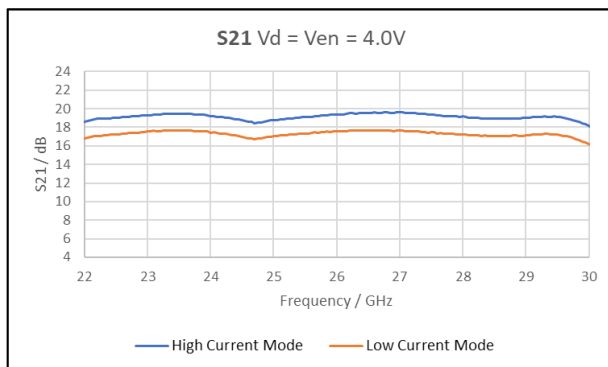
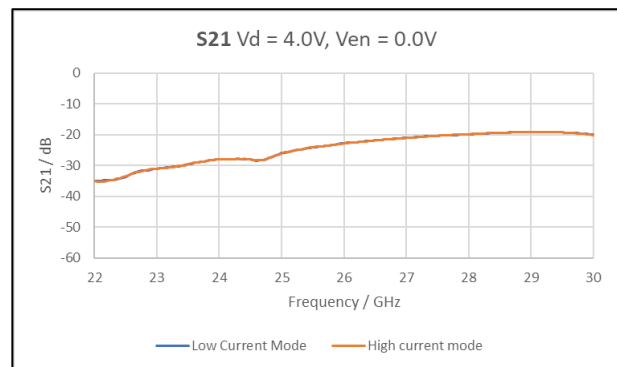
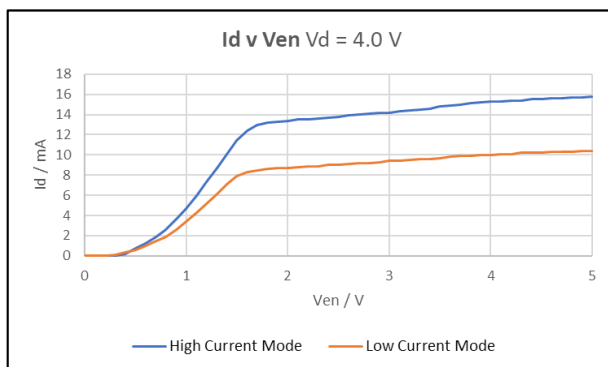
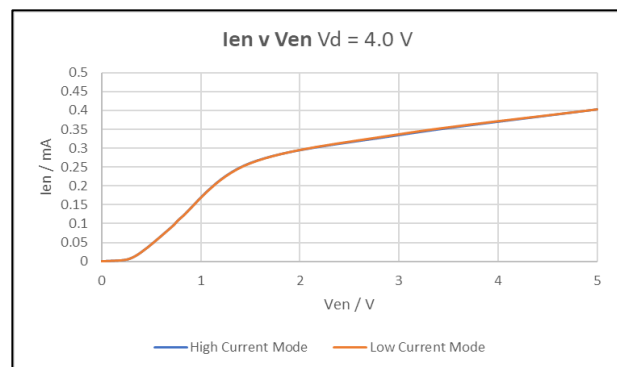
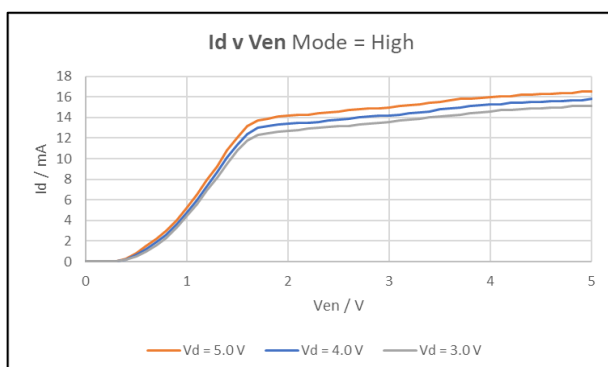
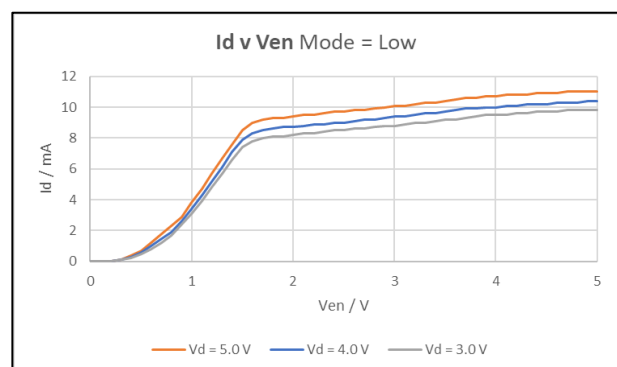
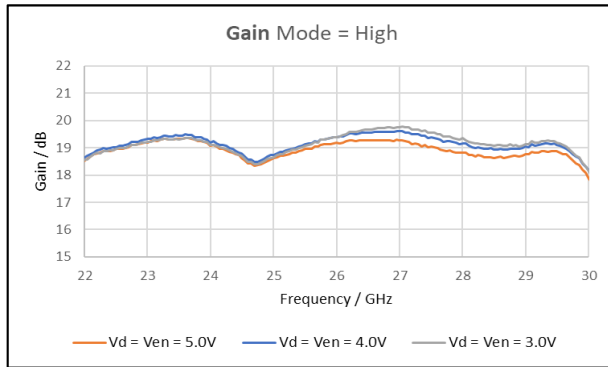
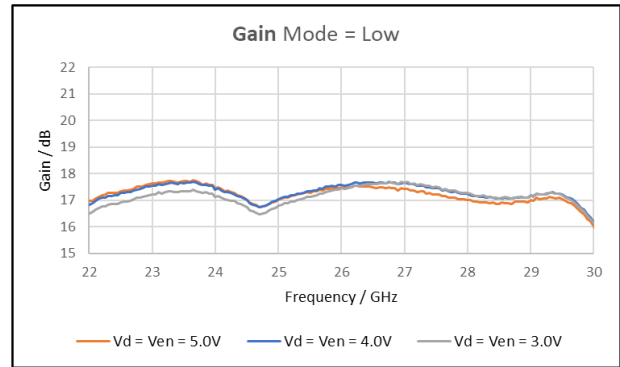
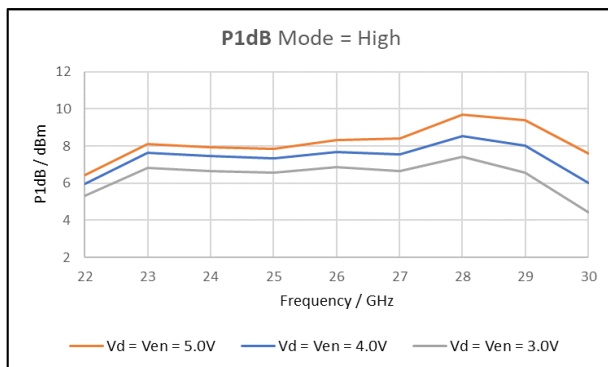
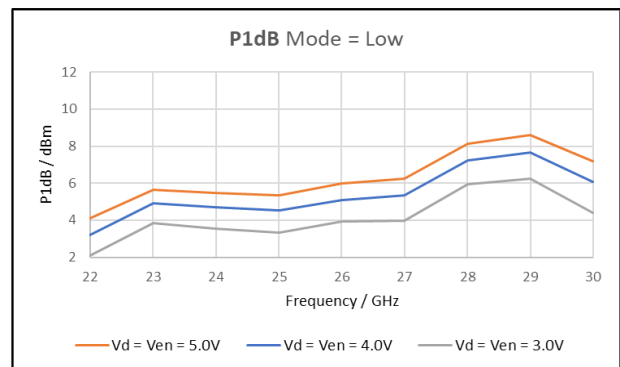
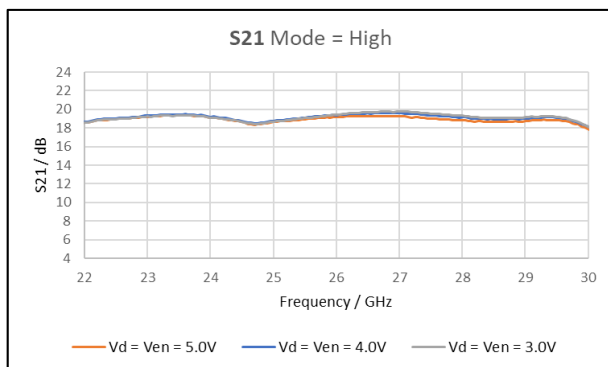
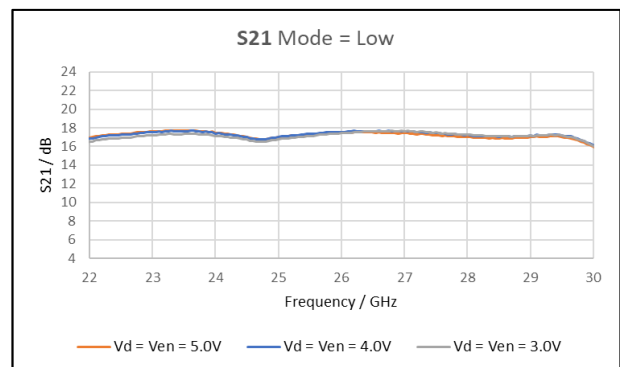
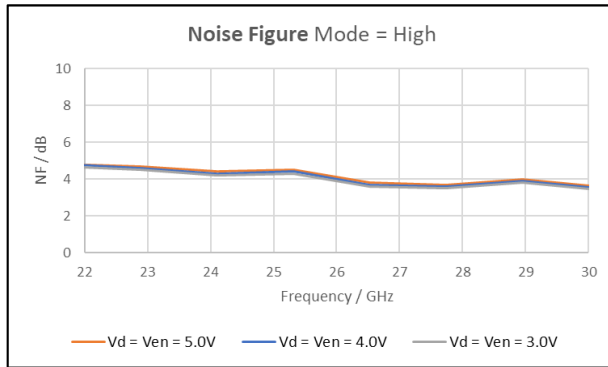
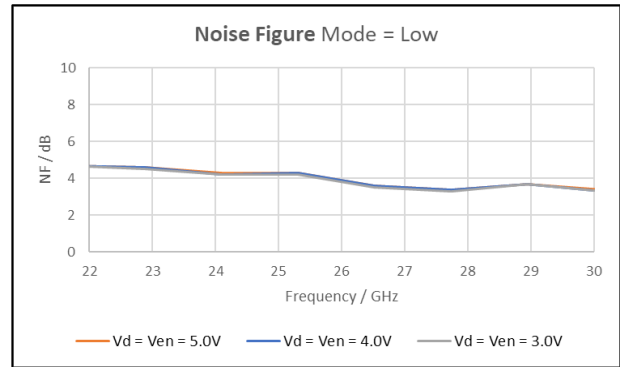
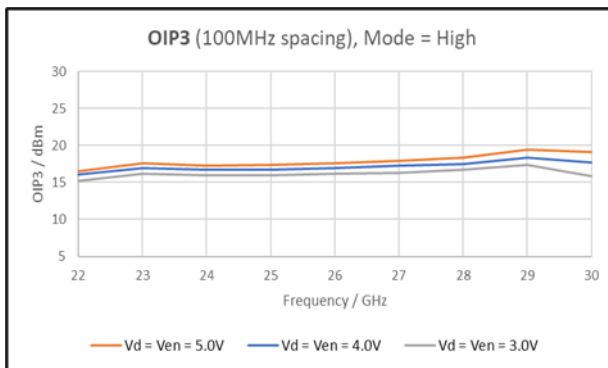
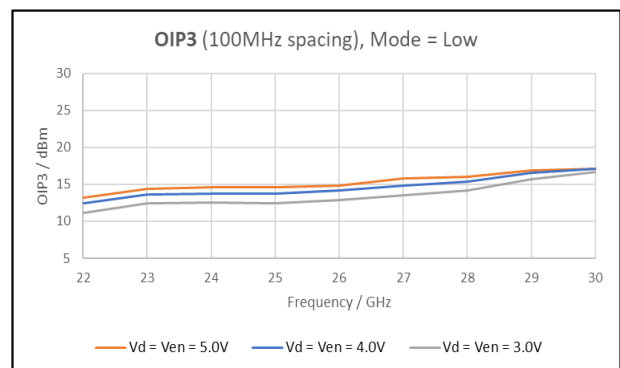
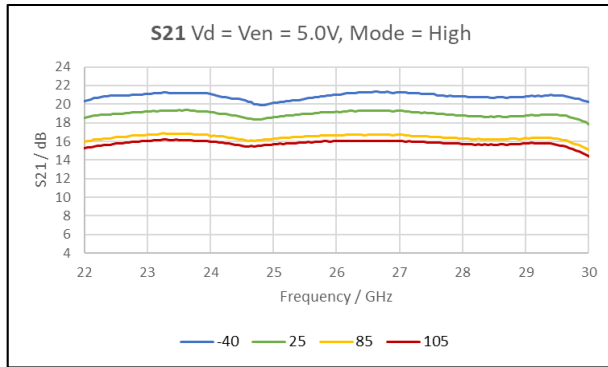
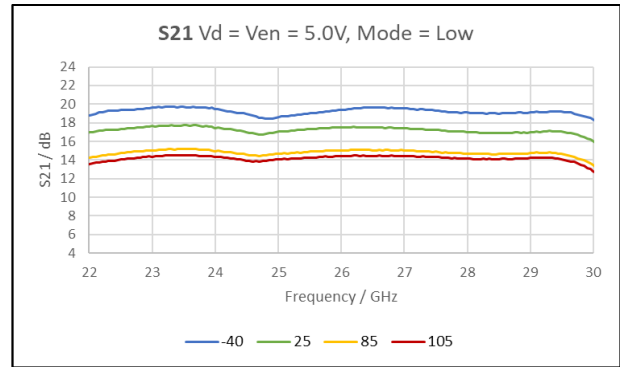
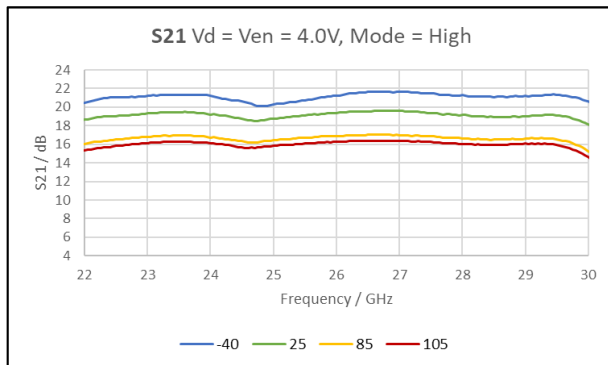
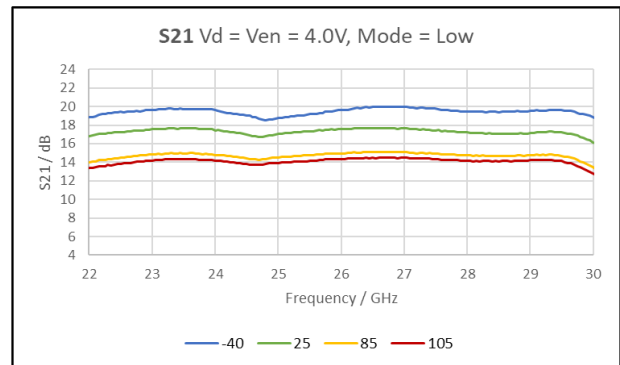
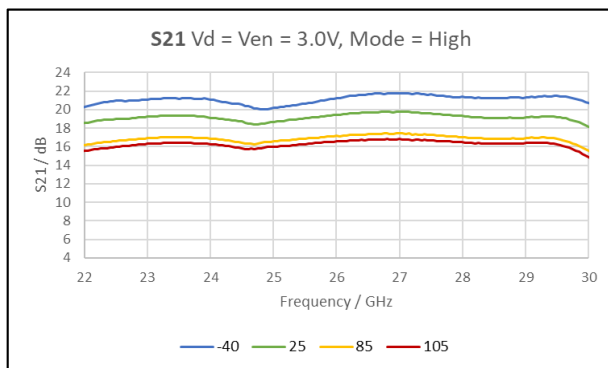
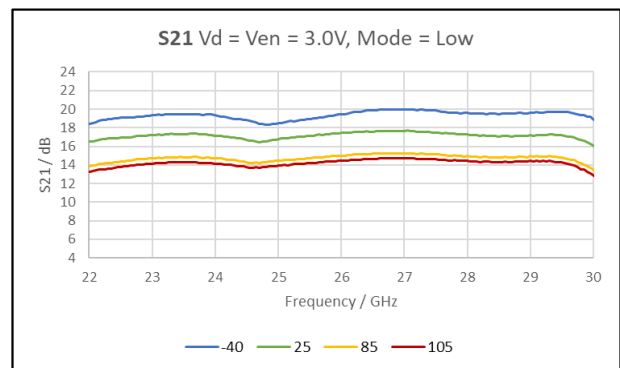
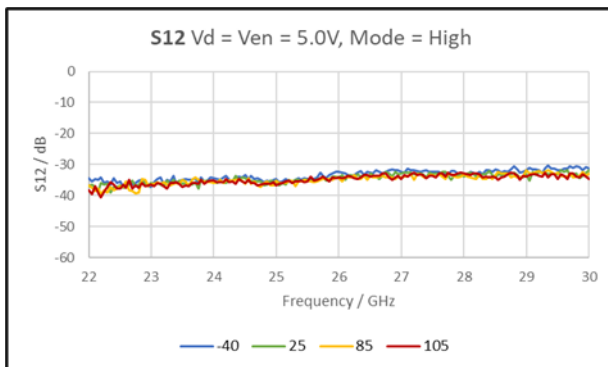
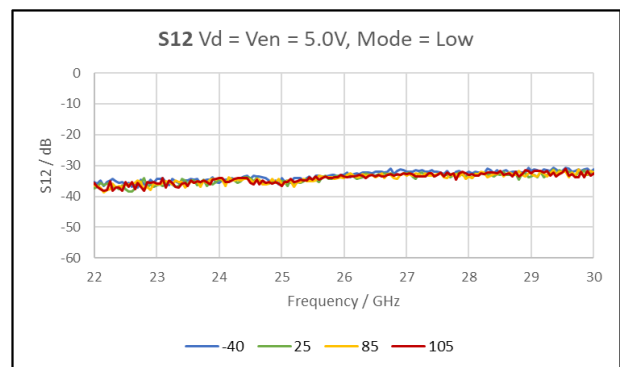


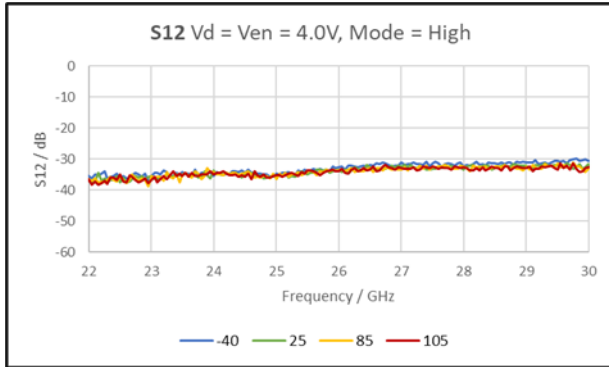
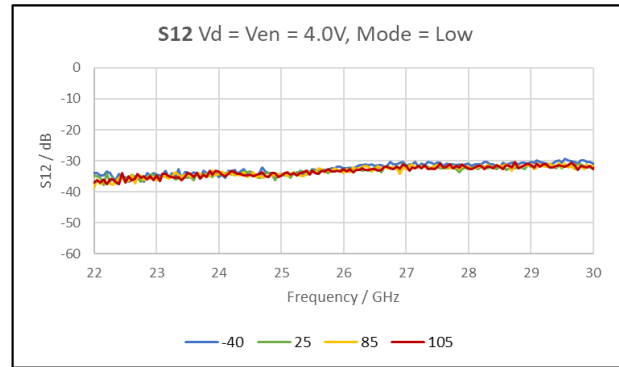
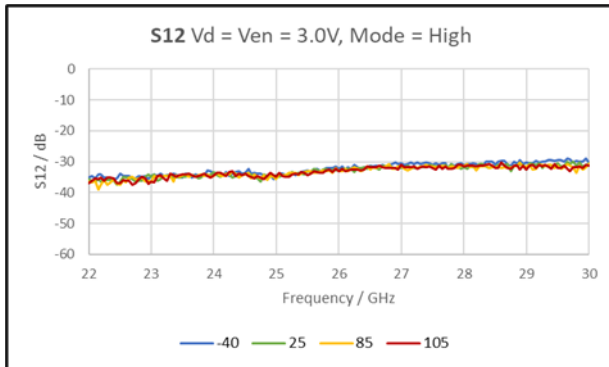
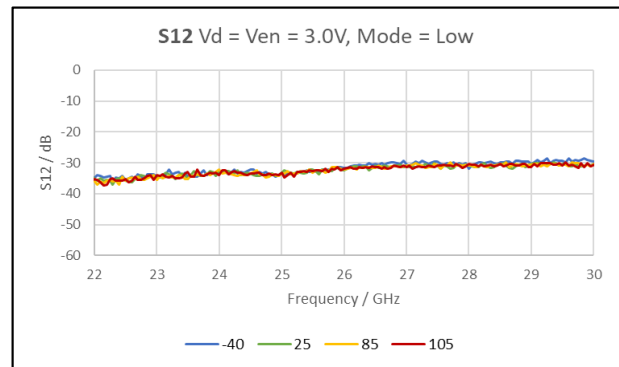
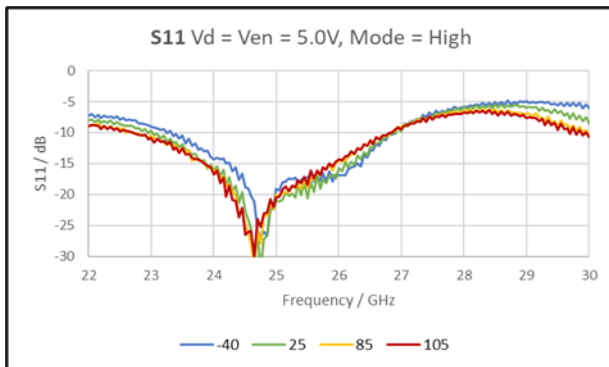
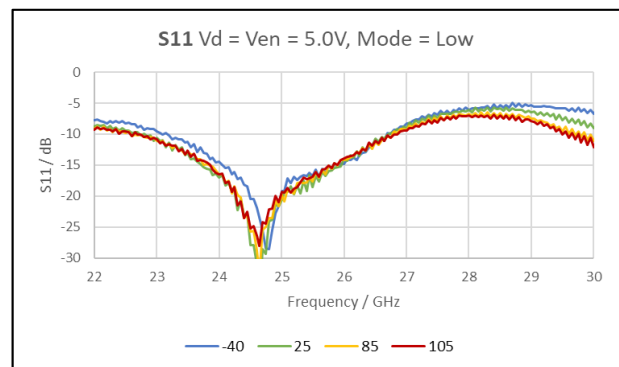
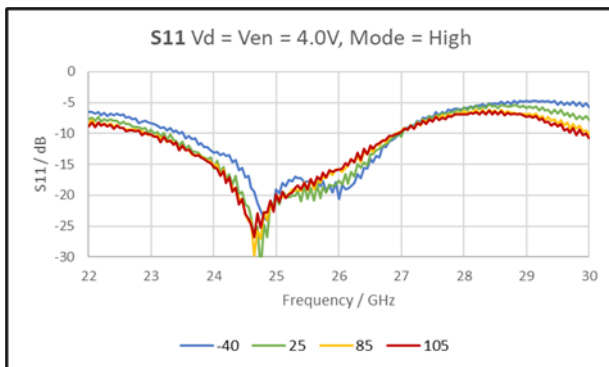
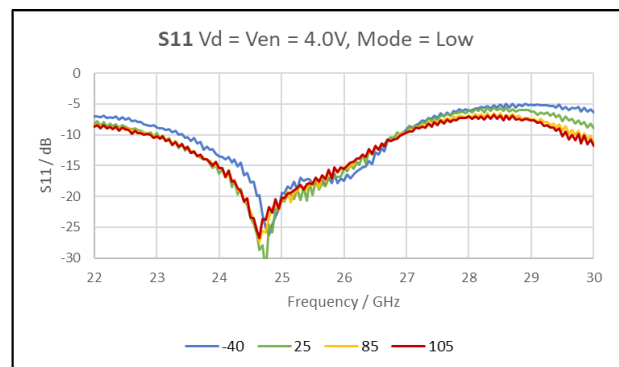
Figure 6: Noise Figure $V_d = V_{en} = 4.0\text{ V}$

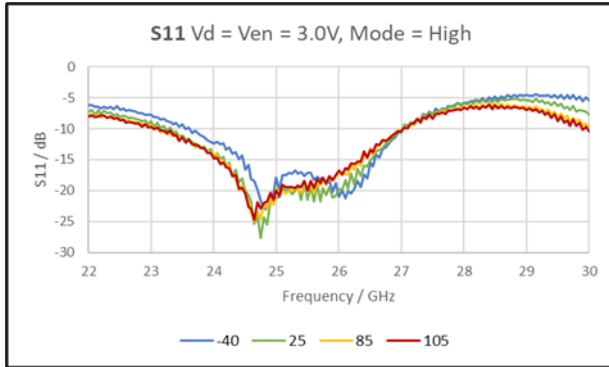
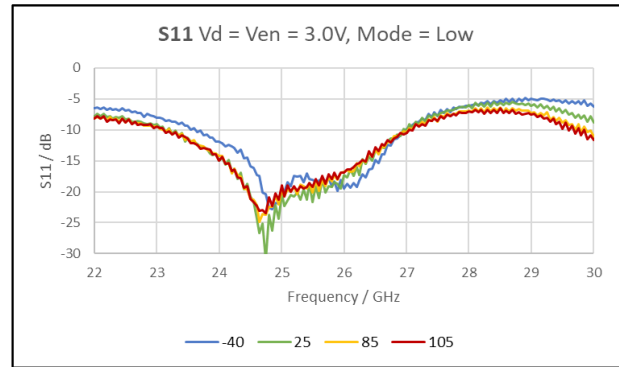
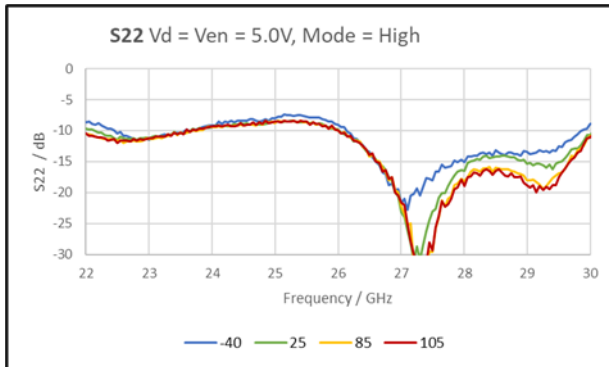
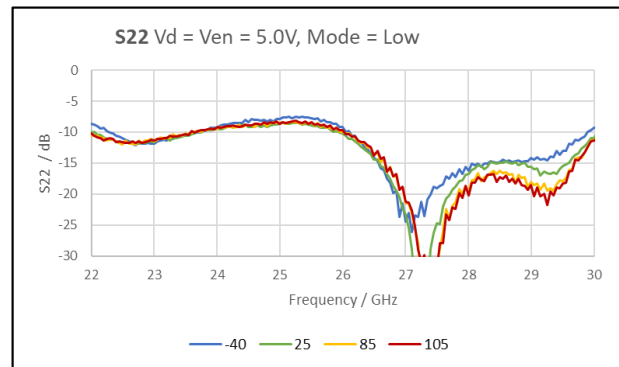
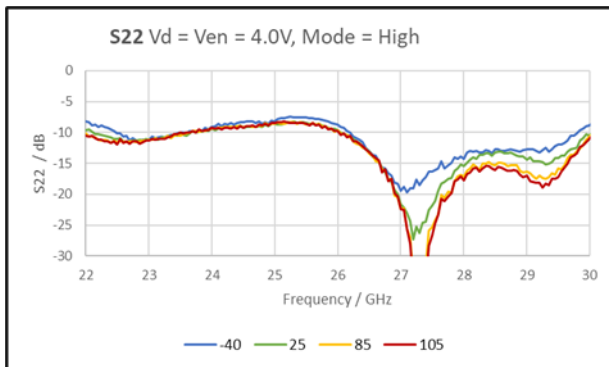
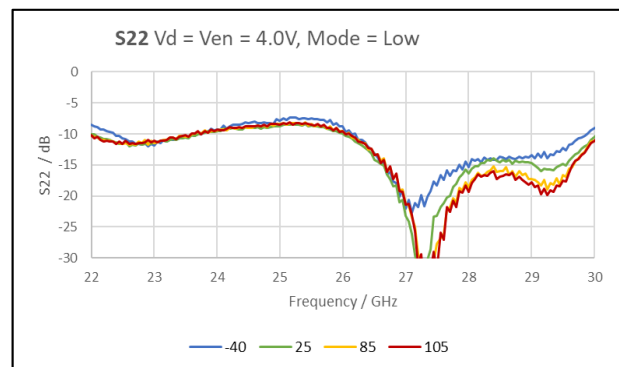
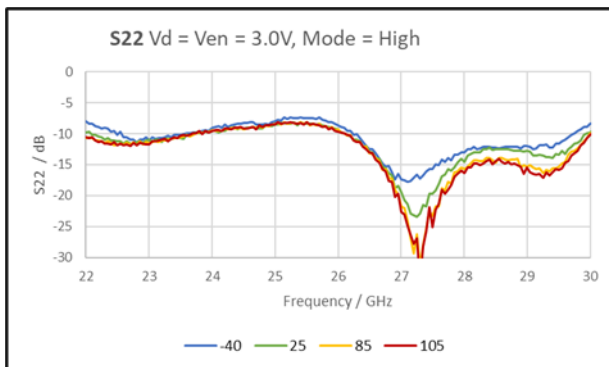
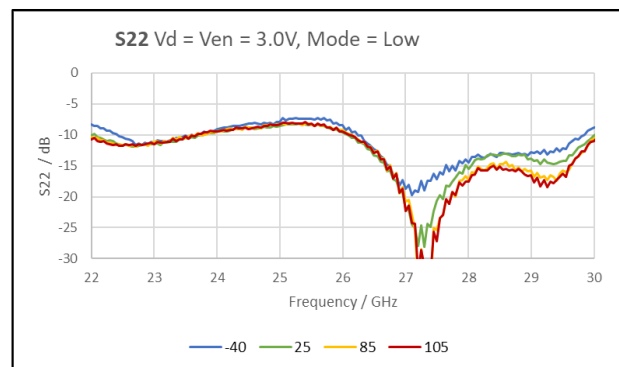
RF typical performance: $V_d = V_{en} = 4.0\text{ V}$, $T_a = 25\text{ }^{\circ}\text{C}$, $Z_0 = 50\text{ }\Omega$ (continued)**Figure 7: Input Return Loss $V_d = V_{en} = 4.0\text{ V}$** **Figure 8: Output Return Loss $V_d = V_{en} = 4.0\text{ V}$** **Figure 9: S_{21} $V_d = V_{en} = 4.0\text{ V}$** **Figure 10: S_{21} $V_d = 4.0\text{ V}$, $V_{en} = 0.0\text{ V}$** **DC typical performance: $V_d = 4.0\text{ V}$, $T_a = 25\text{ }^{\circ}\text{C}$** **Figure 11: I_d v V_{en} $V_d = 4.0\text{ V}$** **Figure 12: I_{en} v V_{en} $V_d = 4.0\text{ V}$** **DC typical performance over voltage: $T_a = 25\text{ }^{\circ}\text{C}$** **Figure 13: I_d v V_{en} , high current mode****Figure 14: I_{en} v V_{en} , low current mode**

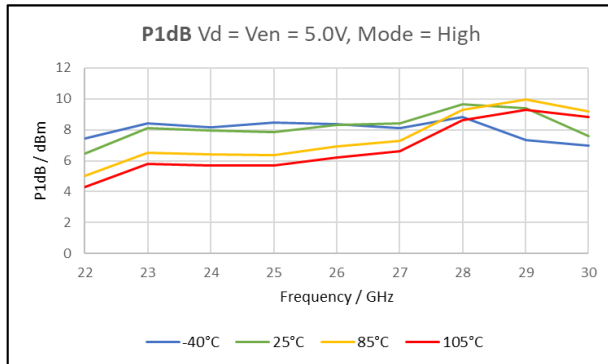
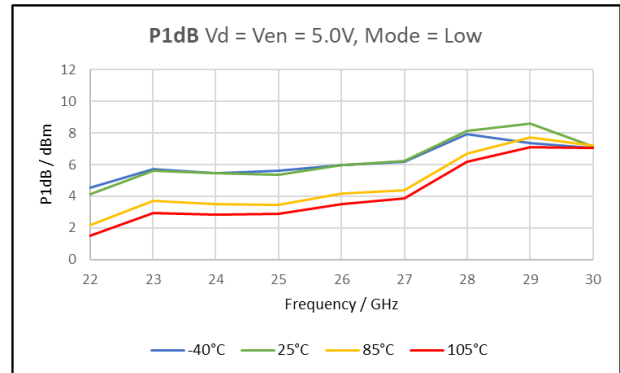
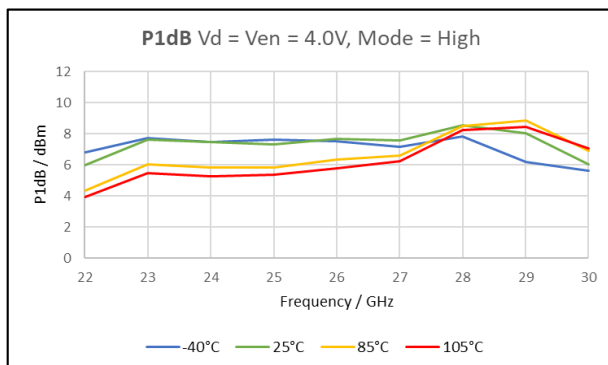
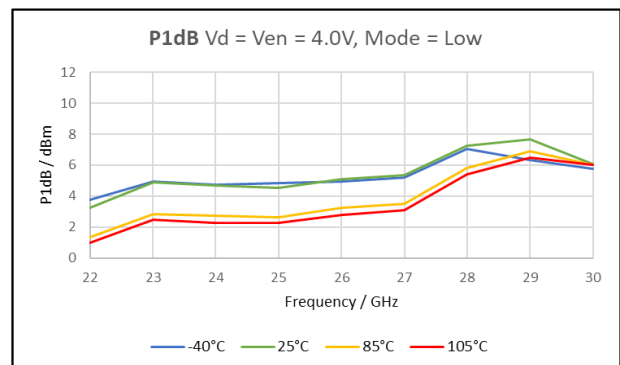
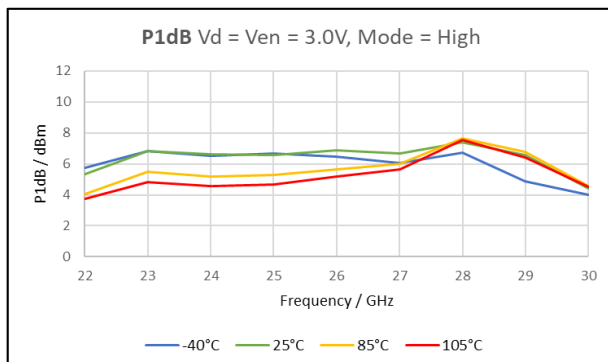
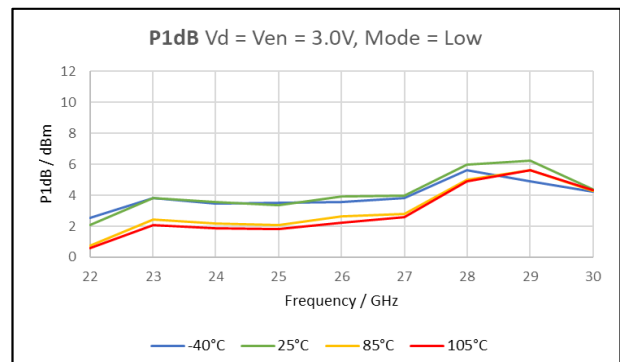
RF Typical Performance over voltage: $V_d = V_{en}$, $T_a = 25^\circ\text{C}$, $Z_0 = 50\ \Omega$ **Figure 15: Gain $V_d = V_{en}$, high current mode****Figure 16: Gain $V_d = V_{en}$, low current mode****Figure 17: P1dB $V_d = V_{en}$, high current mode****Figure 18: P1dB $V_d = V_{en}$, low current mode****Figure 19: S21 $V_d = V_{en}$, low current mode****Figure 20: S21 $V_d = V_{en}$, high current mode**

RF Typical Performance over voltage: $V_d = V_{en}$, $T_a = 25^\circ\text{C}$, $Z_0 = 50\ \Omega$ (continued)**Figure 21: Noise Figure $V_d = V_{en}$, high current mode****Figure 22: Noise Figure $V_d = V_{en}$, low current mode****Figure 23: OIP3 100 MHz spacing, $P_{out} = -7\ \text{dBm}$ / tone, high current mode****Figure 24: OIP3 100 MHz spacing, $P_{out} = -7\ \text{dBm}$ /tone, low current mode**

RF Typical Performance over temperature: $V_d = V_{en}$, $Z_0 = 50\ \Omega$ **Figure 25: S21 $V_d = V_{en} = 5.0\ V$, high current mode****Figure 26: S21 $V_d = V_{en} = 5.0\ V$, low current mode****Figure 27: S21 $V_d = V_{en} = 4.0\ V$, high current mode****Figure 28: S21 $V_d = V_{en} = 4.0\ V$, low current mode****Figure 29: S21 $V_d = V_{en} = 3.0\ V$, high current mode****Figure 30: S21 $V_d = V_{en} = 3.0\ V$, low current mode****Figure 31: S12 $V_d = V_{en} = 5.0\ V$, high current mode****Figure 32: S12 $V_d = V_{en} = 5.0\ V$, low current mode**

RF typical performance over temperature: $V_d = V_{en}$, $Z_0 = 50\ \Omega$ (continued)**Figure 33: S12 $V_d = V_{en} = 4.0\text{ V}$, high current mode****Figure 34: S12 $V_d = V_{en} = 4.0\text{ V}$, low current mode****Figure 35: S12 $V_d = V_{en} = 3.0\text{ V}$, high current mode****Figure 36: S12 $V_d = V_{en} = 3.0\text{ V}$, low current mode****Figure 37: S11 $V_d = V_{en} = 5.0\text{ V}$, high current mode****Figure 38: S11 $V_d = V_{en} = 5.0\text{ V}$, low current mode****Figure 39: S11 $V_d = V_{en} = 4.0\text{ V}$, high current mode****Figure 40: S11 $V_d = V_{en} = 4.0\text{ V}$, low current mode**

RF typical performance over temperature: $V_d = V_{en}$, $Z_0 = 50\ \Omega$ (continued)**Figure 41: S11 $V_d = V_{en} = 3.0\text{ V}$, high current mode****Figure 42: S11 $V_d = V_{en} = 3.0\text{ V}$, low current mode****Figure 43: S22 $V_d = V_{en} = 5.0\text{ V}$, high current mode****Figure 44: S22 $V_d = V_{en} = 5.0\text{ V}$, low current mode****Figure 45: S22 $V_d = V_{en} = 4.0\text{ V}$, high current mode****Figure 46: S22 $V_d = V_{en} = 4.0\text{ V}$, low current mode****Figure 47: S22 $V_d = V_{en} = 3.0\text{ V}$, high current mode****Figure 48: S22 $V_d = V_{en} = 3.0\text{ V}$, low current mode**

RF typical performance over temperature: $V_d = V_{en}$, $Z_0 = 50\ \Omega$ (continued)**Figure 49: P1dB $V_d = V_{en} = 5.0\ V$, high current mode****Figure 50: P1dB $V_d = V_{en} = 5.0\ V$, low current mode****Figure 51: P1dB $V_d = V_{en} = 4.0\ V$, high current mode****Figure 52: P1dB $V_d = V_{en} = 4.0\ V$, low current mode****Figure 53: P1dB $V_d = V_{en} = 3.0\ V$, high current mode****Figure 54: P1dB $V_d = V_{en} = 3.0\ V$, low current mode**

DC typical performance over temperature

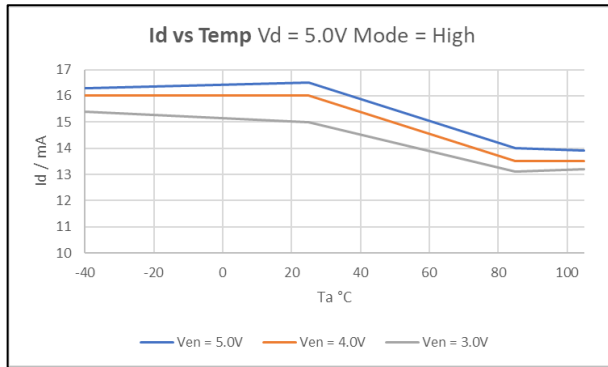


Figure 55: Id v Temp Vd = 5.0 V, high current mode

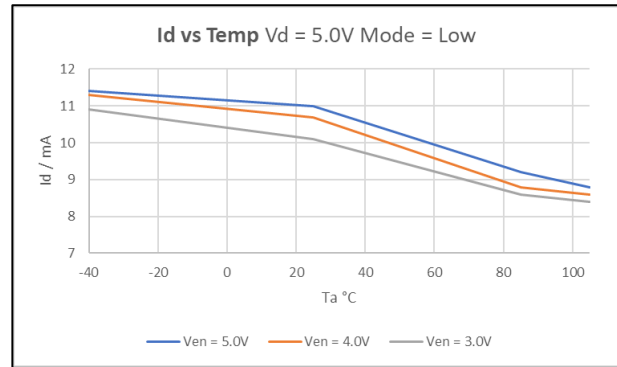


Figure 56: Id v Temp Vd = 5.0 V, low current mode

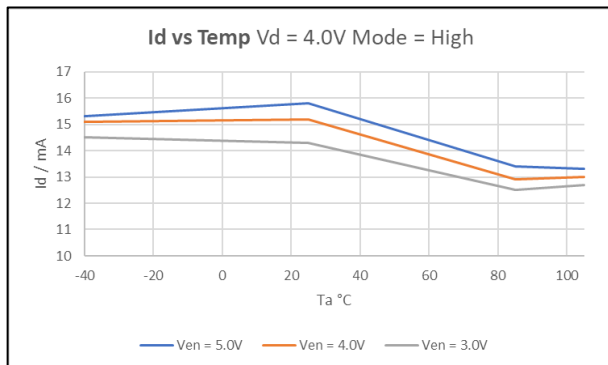


Figure 57: Id v Temp Vd = 4.0 V, high current mode

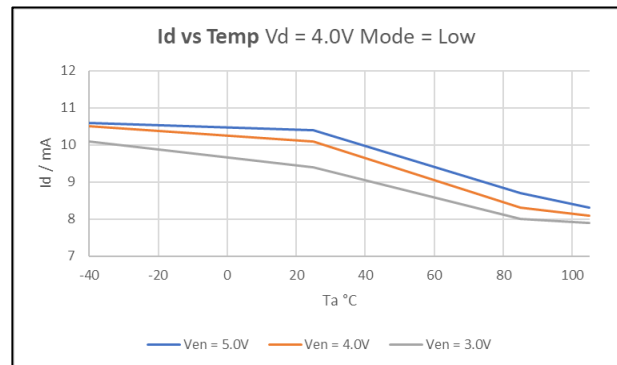


Figure 58: Id v Temp Vd = 4.0 V, low current mode

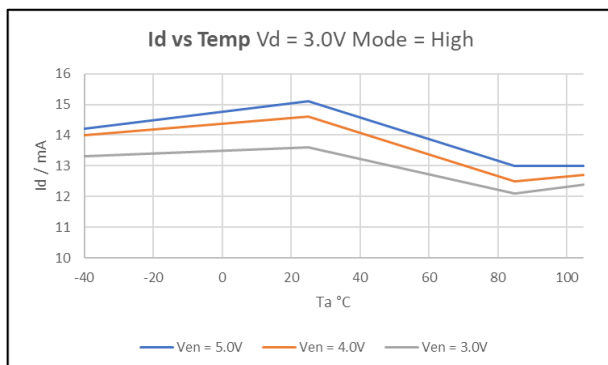


Figure 59: Id v Temp Vd = 3.0 V, high current mode

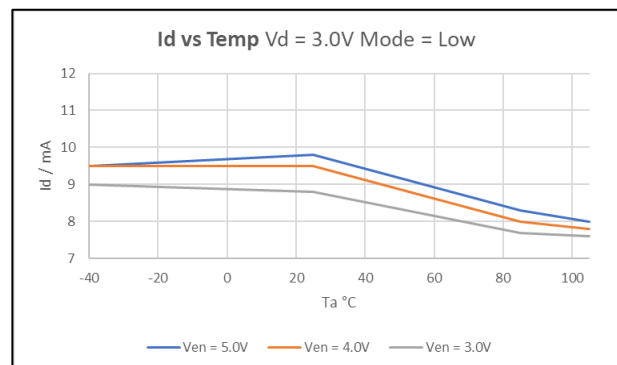


Figure 60: Id v Temp, Vd = 3.0 V, low current mode

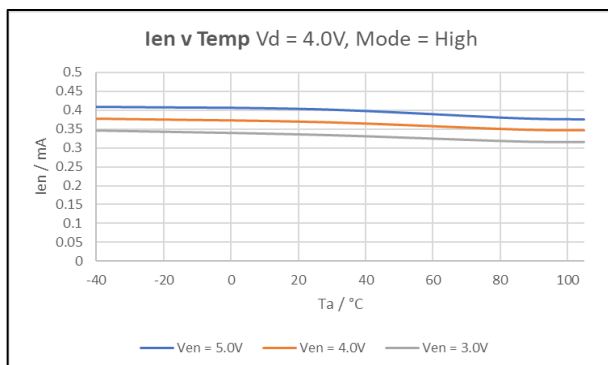


Figure 61: Ien v Temp Vd = 4.0 V, high current mode

Application Information

Schematic Diagram

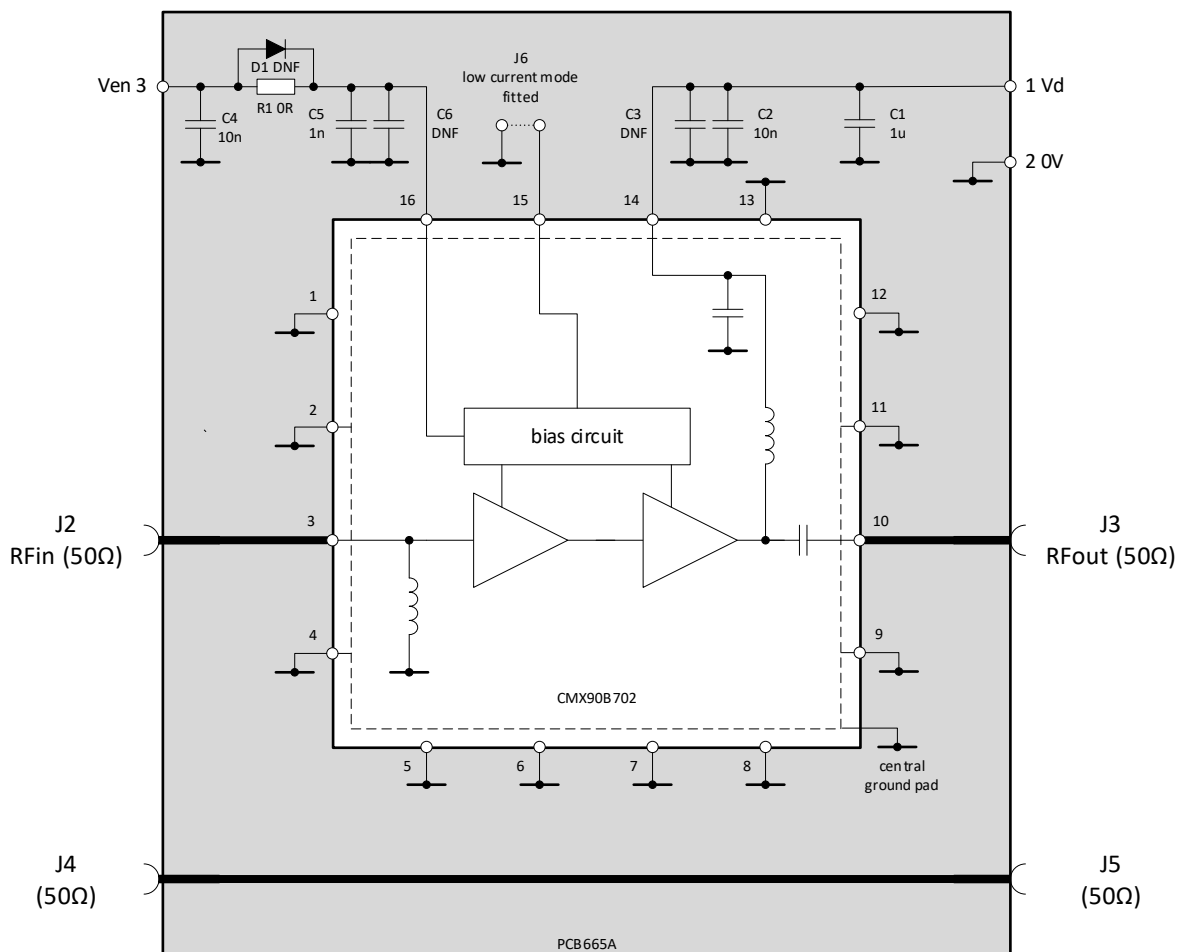


Figure 62: EV90B702 Schematic

Bill Of Materials (BOM)

Reference Designator	Value	Size	Description
C1	1 μ F	0603	16 V, ± 10 %
C2	10 nF	0402	16 V, ± 10 %
C3	DNF	0402	
C4	10 nF	0402	16 V, ± 10 %
C5	1 nF	0402	16 V, ± 10 %
C6	DNF	0402	
R1	0 Ω	0402	0.063 W
D1	DNF	SOD-523F	
J6	N/A	0.1" Header	High / Low Current selection

Notes

- DNF = Do not fit component

PCB Layout

Careful layout of the printed circuit board (PCB) is essential for optimum RF and thermal performance. The recommended layout, including ground via pattern underneath the device, may be taken from the evaluation board (Part Number EV90B702).

The PCB consists of a top layer of MT40 backed by 2 layers of FR-4 with a total thickness of 1.632 mm (Figure 63) and the EV90B702 PCB (Figure 64) is 20 mm x 45 mm. The coplanar RF transmission lines have a width of 0.33 mm with a gap of 0.14 mm to ground either side. The through line length has been reduced by 3mm to account for the length of the device.

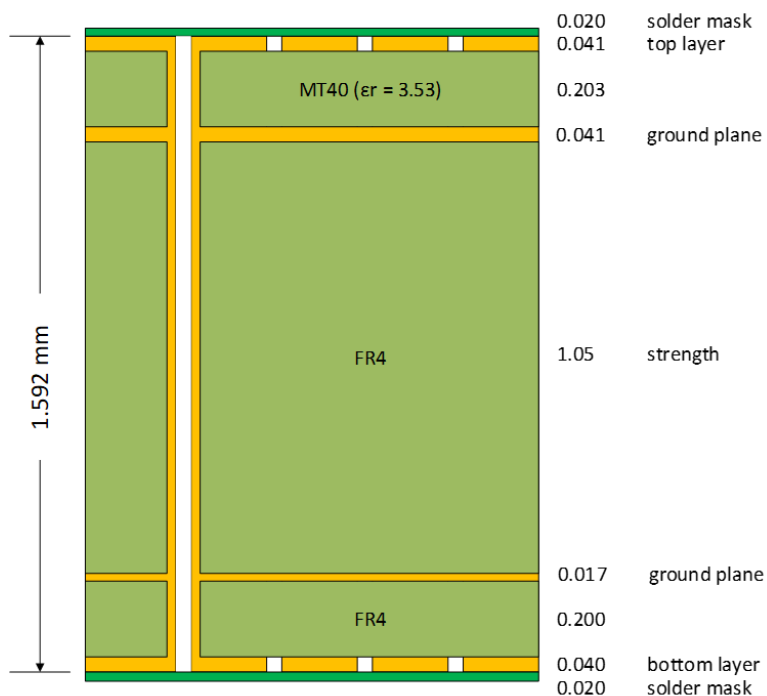


Figure 63: EV90B702 Layer Stack

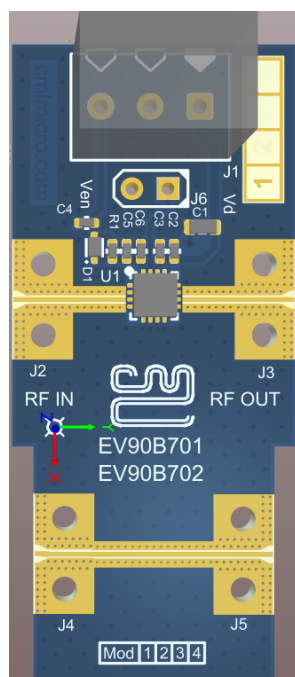


Figure 64: EV90B702 PCB Top Layer View

Thermal Design

The primary RF/DC ground and thermal path is via the exposed die pad on the backside of the package, which must be connected to the PCB ground plane. An array of plated through-hole vias directly underneath the die pad area is essential to conduct heat away and minimise ground inductance. A typical solution will have 9 grounding vias connecting

the top layer to the bottom layer, with inner diameter of 0.2 mm (and 0.025 mm plating) on a 0.55 mm grid pattern. The vias do not need to be filled. The PCB layout should provide a thermal radiator appropriate for the intended operation, adding as much copper to inner and outer layers as possible to avoid excessive junction temperature.

Device junction temperature (T_j) can be calculated using $T_j = T_c + (P_{diss} \times R_{jc})$ where $P_{diss} = P_{dc} + P_{in} - P_{out}$ and T_c is the case temperature on the backside of the package (die pad) in contact with the PCB.

Ven Input

The device is enabled by applying a voltage between 1.8 V and 5.0 V to pin 16 (Ven). The resulting I_d taken by the device is relatively independent of the Ven voltage applied. If the enable feature is not required, the Ven pin can be connected to the same voltage as V_d .

The device can be placed into standby mode when not in use by setting Ven low (<0.2 V) to disable all circuitry.

If lower I_{en} and I_d leakage current and/or if the highest forward isolation is needed in standby mode, a diode can be used in series with the Ven pin to increase the switch-on threshold of the device. This can be particularly important at elevated temperatures. Some suggested diodes in suitable packages (SOD-523F) for the evaluation board are:

- 1N914BWT-D PN fast switching diode
- BAT43XV2-D Schottky diode

Evaluation Board & Bias Procedure

In general, sequencing of the V_d and Ven supplies is not necessary however applying V_d before or simultaneously with Ven is recommended.

The separate through line can be used to measure the evaluation board and connector losses. These results can then be used to de-embed the device performance from evaluation board measurements.

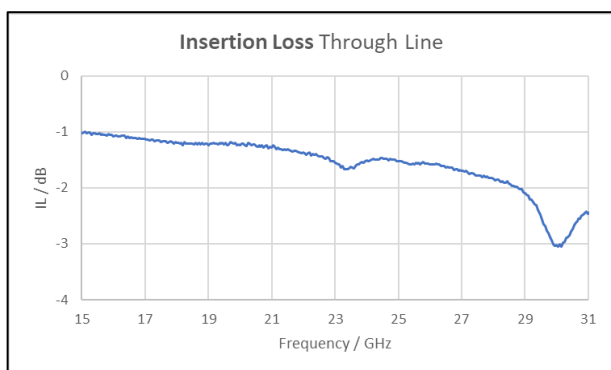


Figure 65: Insertion Loss – through line

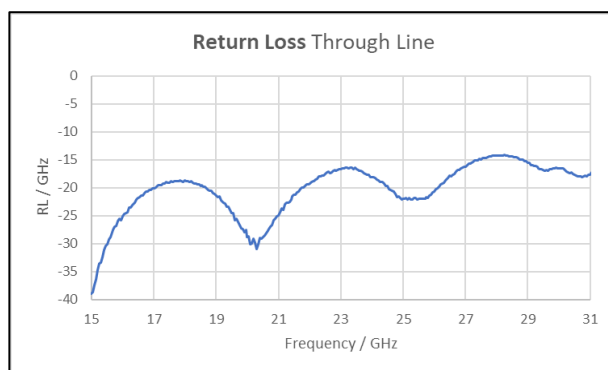


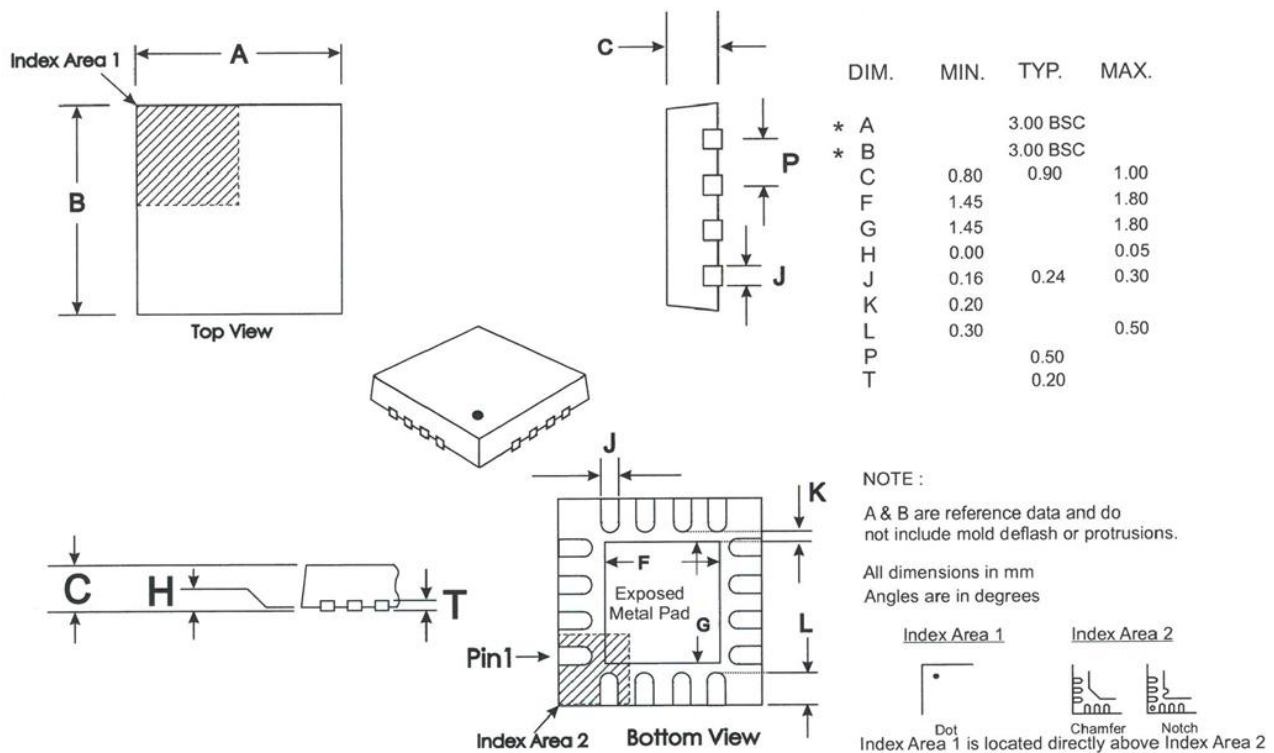
Figure 66: Return Loss – through line

Current Mode Setting

The mode pin (pin 15) is used to set the current taken by the CMX90B702. Low current mode (~10 mA) is selected by fitting the jumper (J6) on the evaluation board, which connects the mode pin to ground. High current mode (~15 mA) is selected by not fitting the jumper, which leaves the mode pin open-circuit.

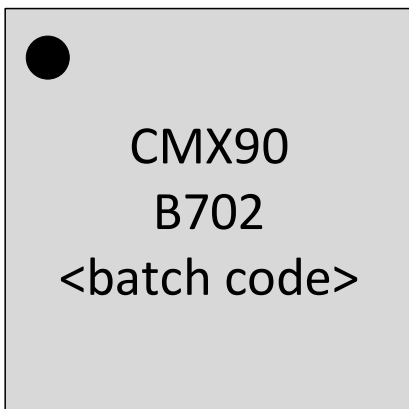
Package Outline

16-lead 3 x 3 mm VQFN Package (QF)



Package Marking

Pin 1 indicator (dot) and 3 rows of text for device identification.



Line 1: CMX90 SμRF series

Line 2: 4-character part code

Line 3: Batch code

Revision History

Issue	Description	Date
1	First release for product launch	March 2023

ROHS Compliance



CML Micro certifies, to the best of our knowledge, that its products comply with **RoHS directive (2011/65/EU)**, as amended by **Directive (EU) 2015/863**.

REACH Compliance



CML Micro certifies, to the best of our knowledge, that its products do not contain any of the banned substances specified in the SVHC list at <https://echa.europa.eu/candidate-list-table>. CML Micro are committed to ensuring the safety of products and the compliance with regulations. Publications will be updated in the event that REACH control is compromised.

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