



**SICOMM**

# SCT3288 Advanced Baseband Processor

## Advanced Baseband Processor

D3288/3 June 2023

## DATASHEET

Advance Information

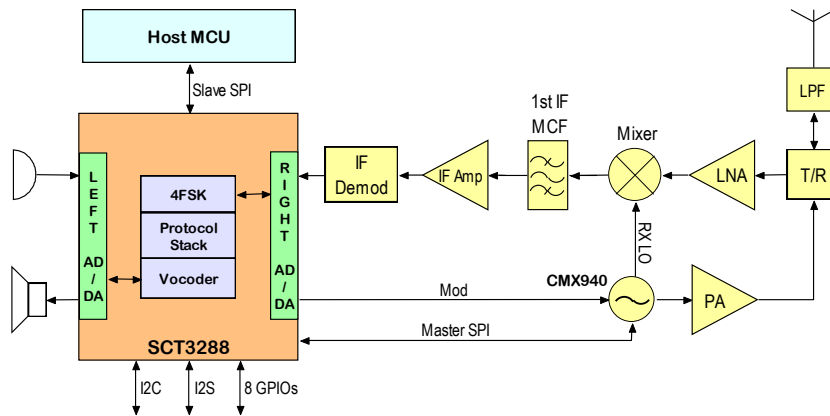
### Features

- Low power 4FSK modem
- Digital PMR protocol engine
- Integrated vocoder
  - Standards compliant AMBE+2™
  - Other 2400bps options
- Integrated RF and audio interfaces
  - 24-bit ADC/DACs
- Flexible receiver support
  - I/Q or superhet

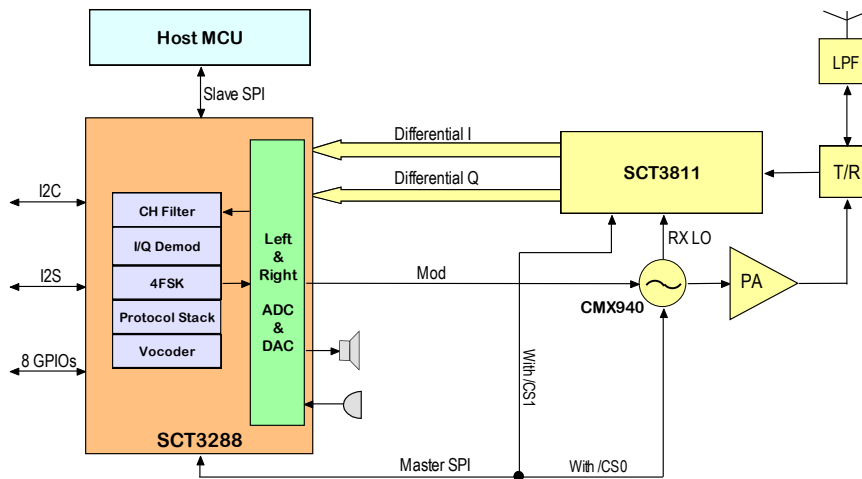
- Noise and anti-howl suppression
- Digital and analog PMR support
  - With auto mode detection
- Single 3.3V supply
  - On chip step down regulator for core supply
- 88QFN package

### Applications

- Dual mode PMR radios
- Dual mode PMR modules
- FSK data modems



DMR/dPMR System with Conventional RF



DMR/dPMR System with SCT3811

## 1 Brief Description

The SCT3288 is a low power high performance baseband processor supporting dPMR and DMR protocol. With an internal codec (audio band ADC and DAC), it completes the entire physical layer and data link layer, and most of the call control layer processing of dPMR and DMR protocols. In dPMR mode, SCT3288 complies with ETSI TS 102 490 and ETSI TS 102 658. In DMR mode, it complies with ETSI TS 102 361. The two front page diagrams show the SCT3288 used in a dPMR or DMR system with conventional RF circuits and used with the SCT3811 single conversion receiver. The SCT3288 is designed for easy migration from analog radios. The system designer can start with a typical analog radio, replacing the analog baseband processor with the SCT3288, to obtain the simplest form of a dPMR or DMR radio. To achieve the full potential of dPMR or DMR, application-level software programming is required on the host processor.

The SCT3288 contains an I2S interface, a slave SPI interface, a master SPI interface with two chip selectors, an I2C interface and 8 programmable I/O ports. The I2S is used for connection with an external codec or a receiver with digital I/Q interface. The master SPI can be used to control the RF PLL or a transceiver such as CMX940 and SCT3811.

The SCT3288 communicates with a host processor through the slave SPI interface. The firmware of the SCT3288 is stored on chip. The SCT3288 gives a response to the host processor to indicate that it has started up successfully and is ready to accept commands from the host processor. Following a correct command from the host the SCT3288 will then load and execute the entire firmware.

The SCT3288 core logic operates at 1.2 V, and the I/O operates at 1.8-3.6V. The SCT3288 is supplied in a QFN88 10x10mm<sup>2</sup> and 0.4mm pitch, ideal for small form factor designs.

The SCT3288 provides:

### DMR

- Supports DMR Tier1 and Tier 2 (ETSI TS 102 361)
- Air interface physical layer (layer 1)
- Air interface data link layer (layer 2)
- Air interface call control layer (layer 3)
- Annex C (TS 102 361-2) support, with BCD addressing and automatic call match
- Transmit in slotted or continuous mode
- Receive in slotted or continuous mode
- Support TDMA direct mode

### dPMR

- Supports dPMR Tier 1 (ETSI TS 102 490)
- Supports dPMR Tier 2 (ETSI TS 102 658) Mode 1 and Mode 2
- Air interface physical layer (layer 1)
- Air interface data link layer (layer 2)
- Air interface call control layer (layer 3)
- Full Annex A support, with BCD addressing and automatic call match

### 4 FSK Modem

- 4800 bps data rate for dPMR and 9600 bps for DMR
- Automatic frame sync detection
- Programmable modulation index
- Support two-point modulation, and I/Q modulation
- BER Test Mode complied with ITU O.153

### Vocoder

- Built-in AMBE+2™ vocoder from DVSI
- Supports 1031 Hz Tone and Silence Test Mode

### Analog Mode Support

- Supports voice channel filters (LPF/HPF/Limiter), as well as pre-emphasis and de-emphasis filters
- Supports CTCSS/DCS generation and detection
- Supports arbitrary CTCSS/DCS code, and blind detection
- Supports the non-standard 55 Hz CTCSS tail tone
- Supports compander

- Automatic mode detection (analog and dPMR or analog & DMR) in receiver mode

**Digital interfaces**

- 1 x I2S
- 1 x I2S\_Tx only
- 1 x I2S\_Rx only
- 1 x Slave SPI
- 1 x Master SPI with two chip selectors
- 1 x I2C
- 8 x programmable I/O
- 1 x UART

**Clock Generation Unit**

- The clock circuit can operate with either a crystal or external clock generator

**Power Supply**

- On-chip LDO generates 3.0V for internal analog circuits (except Codec) power supply.
- On-chip DC/DC generates 1.2V for core power supply.
- An external dedicated 3.3V analog power supply for the internal codec.
- A dedicated IO power supply, of 1.8V to 3.6V.

**Codec**

- Two channel 24-bit sigma-delta ADC and DAC.
- Audio PLL.
- Two differential inputs and 2 single-ended inputs.
- Two pairs of line outputs
- Programmable analog and digital gain

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**History**

Version	Changes	Date
3	Limited Production release	June 2023
2	First public launch	November 2021
1	First release, Advance Information	June 2020

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document.

## 2 Block Diagram

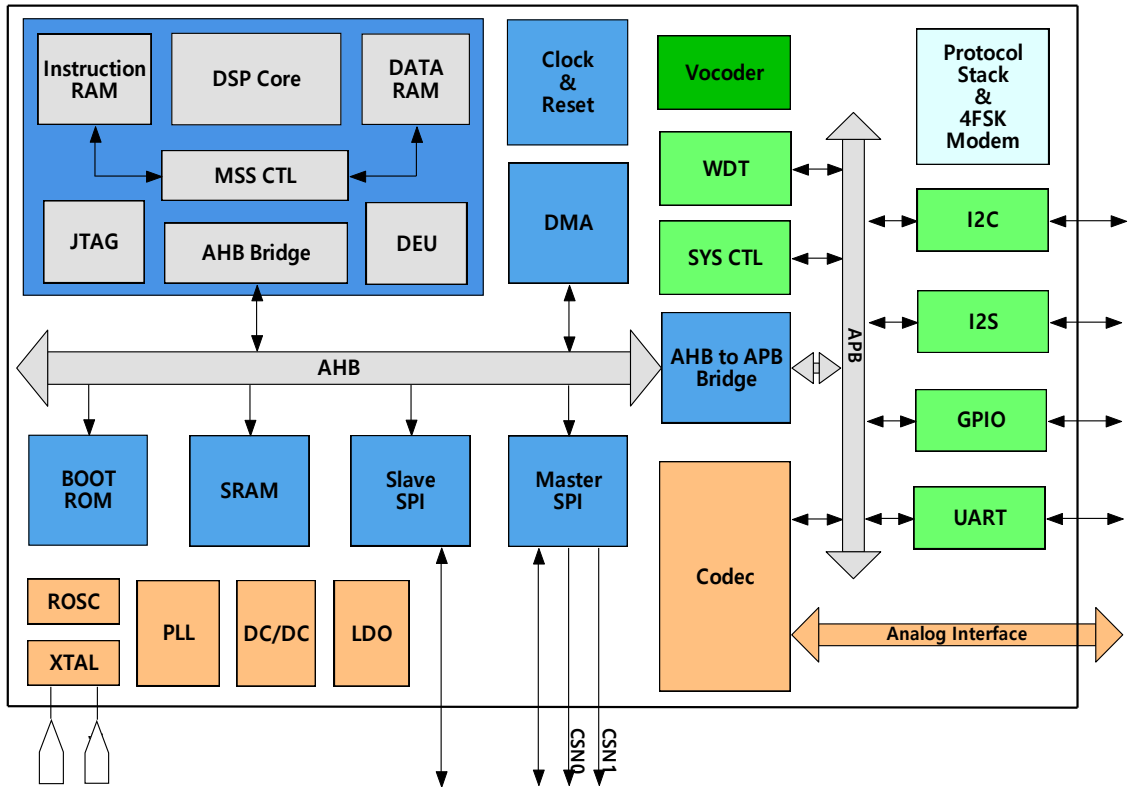


Figure 1 SCT3288 Block Diagram



### 3 Performance Specification

#### 3.1 Electrical Performance

##### 3.1.1 Absolute Maximum Ratings – typical figures

Exceeding these maximum ratings can result in damage to the device.

Parameter	Min.	Max.	Unit
AV33 to AVSS	-0.3	3.9	V
DV33 to DVSS	-0.3	3.9	V
AVDD to AVSS	-0.3	3.9	V
VDD to VSSD	-0.3	1.5	V
AV12_PLL to AVSS	-0.3	1.5	V
VDDIO to VSSD	-0.3	3.9	V
Voltage on any pin to VSSD	-0.3	VDDIO+0.3	V
Voltage on any pin to AVSS	-0.3	AV33+0.3	V
Operating temperature range	-40	85	°C
Storage Temperature	-55	125	°C
Total Power Dissipation at Tamb = 25°C	-	3500	mW/°C

##### 3.1.2 Operating Limits

Correct operation of the device outside these limits is not implied. The typical value is recommended.

Parameter	Note	Min.	Typ	Max.	Unit
AV33_DC/DC to AVSS		1.7	3.3	3.6	V
DV33_DC/DC to DVSS		1.7	3.3	3.6	V
AV33_PRG to AVSS		3.0	3.3	3.6	V
AVDD_CODEC to AVSS		3.0	3.3	3.6	V
AVDD to AVSS	1	2.7	3.0	3.6	V
VDD to VSSD	2	1.08	1.2	1.32	V
AV12 to AVSS	2	1.08	1.2	1.32	V
VDDIO to VSSD		1.8	-	3.6	V
XTAL Frequency		12.8	19.2	26	MHz
External Clock Frequency		12.8	19.2 / 38.4	40	MHz
System Clock Frequency			153.6	200	MHz
Operating temperature range		-40	25	85	C

Note:

1. AVDD comes from the on-chip LDO
2. The power supply comes from the on-chip DC/DC

### 3.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

At 25 °C, AV33 = DV33 = VDDIO = 3.3V, AVDD = 3.0V (powered by on-chip LDO), VDD = 1.2V (powered by on-chip DC/DC). System clock is 153.6 MHz, and the codec sample rate is 24 kHz. Unused peripheral interface in typical application scenario (I2S\_R and I2S\_T) is disabled.

Supply Current					
Parameter	Comment	Min	Typ	Max	Unit
Normal mode					
VDD	(Note 1)		24.1		mA
AV12_PLL			0.52		mA
AVDD_PLL			0.5		mA
AVDD_ROSC			13		uA
VDDIO			0.88		mA
Sleep Mode					
VDD	(Note 1)		0.57		mA
AV12_PLL			1.3		uA
AVDD_PLL			<1		uA
AVDD_ROSC			13		uA
VDDIO			0.8		mA
Halt Mode					
VDD	(Note 1)		0.56		mA
AV12_PLL			1.3		uA
AVDD_PLL			<1		uA
AVDD_ROSC			13		uA
VDDIO			0.8		mA
Digital Interface Logic					
Logic Input					
V <sub>IH</sub>	VDDIO = 3.3V	2			V
V <sub>IL</sub>	VDDIO = 3.3V			0.8	V
V <sub>IH</sub>	VDDIO = 2.5V	1.7			V
V <sub>IL</sub>	VDDIO = 2.5V			0.7	V
V <sub>IH</sub>	VDDIO = 1.8V	1.05			V
V <sub>IL</sub>	VDDIO = 1.8V			0.69	V
Logic Output					
V <sub>OH</sub>	VDDIO = 3.3V,	2.4			V
V <sub>OL</sub>	I <sub>o</sub> = 4 mA			0.4	V
V <sub>OH</sub>	VDDIO = 2.5V,	1.7			V
V <sub>OL</sub>	I <sub>o</sub> = 2mA			0.7	V
V <sub>OH</sub>	VDDIO = 1.8V,	1.17			V
V <sub>OL</sub>	I <sub>o</sub> = 2mA			0.45	V
On-chip DC/DC					
Input Voltage Range Vin		1.7	3.3	3.6	V
Output Voltage Vout		1.08	1.2	1.32	V
Efficiency η	SCT3288 Works in normal mode @ 3.3V input		76		%
Maximum Output Current				300	mA
On-chip LDO					
Input Voltage Range Vin		3.0	3.3	3.6	V
Output Voltage Vout	Vin ≥ 3V+Vdrop		3.0		V
	3V < Vin < 3V+Vdrop <sup>(2)</sup>		Vin-Vdrop		V
Dropout Voltage Vdrop			250		mV
Output Accuracy	When Vout = 3V		+/-10		%
Output Current Iout				200	mA
Codec					
Power Supply Range AVDD_CODEC		3.0	3.3	3.6	V
Supply current I <sub>AVDD</sub> Normal mode	DAC&ADC, LOUT1, ROUT2 and DEMOD_IN active		16.1		mA

Supply current $I_{AVDD}$ Sleep mode	All blocks powered down except Vref	0.3		mA
Supply current $I_{AVDD}$ Deep Sleep mode	All blocks powered down		<1	$\mu$ A
VMID		0.5*AVDD		V
<b>Microphone Bias</b>				
Bias Voltage		0.75*AVDD		V
Maximum Output Current			3	mA
Capacitive Load			50	pF
<b>Line Input</b>				
Resolution		24		bit
THD (Total Harmonic Distortion)	(Note 3)	-82	-70	dB
Dynamic Range (-60dB input, A-weighted)	(Note 4)	96		dB
S/N (A-weighted)	(Note 5)	80	96	dB
Channel Separation	(Note 6)	100		dB
Channel Matching		0.2		dB
Full Scale Input Voltage Single-ended $V_{FS}$		AVDD		Vpp
Differential $V_{FS}$		2*AVDD		Vpp
Input Impedance		10		kohm
Input Capacitor		50		pF
<b>ADC Digital Filter</b>				
Passband		0.4		fs
Passband Ripple		+/- 0.05		dB
Stopband	0.6			fs
Stopband Attenuation	>0.583 fs	-78		dB
<b>Line output</b>				
THD (Total Harmonic Distortion)	(Note 3)	-80	-70	dB
Dynamic Range (-60dB input, A-weighted)	(Note 4)	98		dB
S/N (A-weighted)	(Note 5)	85	98	dB
Channel Separation	(Note 6)	100		dB
Channel Matching		0.2		dB
Full Scale Output Voltage		0.875*AVDD		Vpp
Load Resistance		10		kohm
Load Capacitor			50	pF
<b>DAC Digital Filter</b>				
Passband		0.444		fs
Passband Ripple		+/- 0.05		dB
Stopband	0.556			fs
Stopband Attenuation	>0.583 fs	-60		dB

## Note:

- Does not include codec (AVDD\_CODEDC), PLL analog and ROOSC (ring oscillator) analog power
- Not recommended.
- THD is the Distortion/Signal ratio calculated with rms values.
- Dynamic range is a measure of the difference between the highest and lowest portions of a signal. Normally a THD + N measurement at 60 dB is below full-scale. The measured signal is then corrected by adding 60dB (e.g. THD + N @ -60dB = -32 dB, DR = 92 dB).
- SNR is a measure of the difference between the full-scale output and the output with no signal applied.
- Channel Separation also is known as crosstalk, which measures how good one channel is isolated from another channel. Normally it is done by sending a full-scale signal to one channel and measuring the other.

### 3.2 Slave SPI Timing

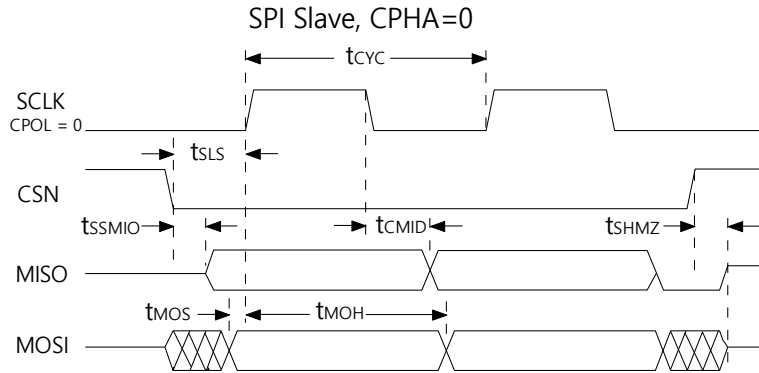


Figure 2 Slave SPI Timing

SPI Slave Timings	Notes	Min.	Typ.	Max.	Units
$t_{CYC}$	SCLK cycle time	500	-	-	ns
$t_{SSMIO}$	CSN to MISO output	3.8	-	12	ns
$t_{SLS}$	CSN to SCLK setup	$t_{CYC} / 2$	-	-	ns
$t_{CMID}$	SCLK to MISO delay	3	-	12	ns
$t_{MOS}$	MOSI to SCLK setup	4	-	-	ns
$t_{MOH}$	MOSI to SCLK hold	1.3	-	-	ns
$t_{SHMZ}$	CSN to MOSI and MISO tri-state	3.8	10	12	ns

### 3.3 I2S Timing

#### 3.3.1 I2S Timing in Slave Mode

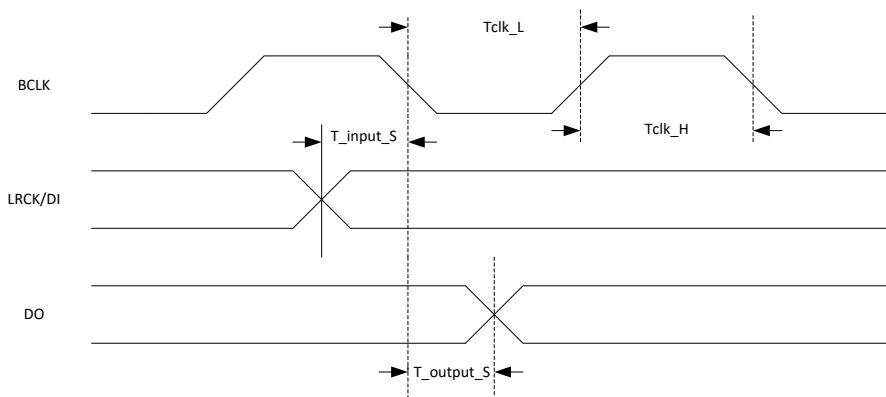


Figure 3 I2S Timing in Slave Mode

Parameter	Description	Min.	Typ.	Max.	Units
Tclk_L	BCLK low level	68.5	-	-	ns
Tclk_H	BCLK high level	68.5	-	-	ns
T_input_S	LRCK/DI to BCLK setup	-	-	26	ns
T_output_S	BCLK to DO setup	-	-	27	ns

### 3.3.2 I2S Timing in Master Mode

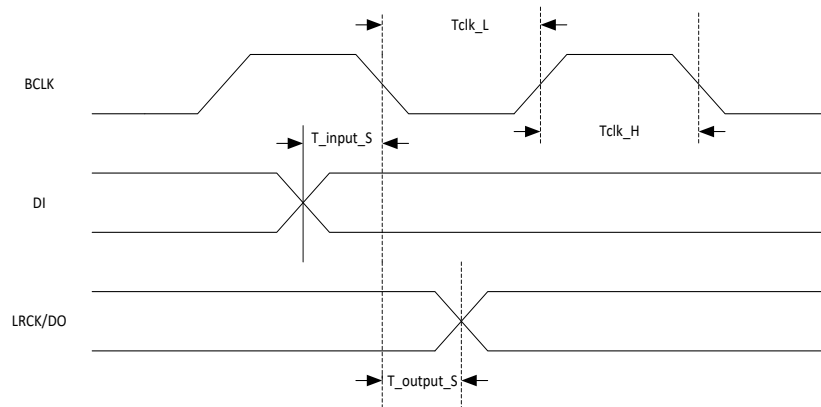


Figure 4 I2S Timing in Master Mode

Parameter	Description	Min.	Typ.	Max.	Units
Tclk_L	BCLK low level	40	-	-	ns
Tclk_H	BCLK high level	40	-	-	ns
T_input_S	DI to BCLK setup	-	-	16	ns
T_output_S	BCLK to DO/LRCK setup	-	-	10	ns

### 3.4 Master SPI Timing

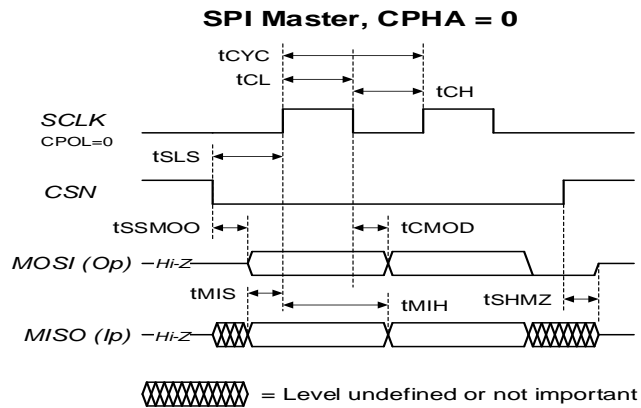


Figure 5 Master SPI Timing

SPI Master Timings	Min.	Typ.	Max.	Units
t <sub>CYC</sub>	40	-	-	ns
t <sub>CL</sub>	-	20	-	ns
t <sub>CH</sub>	-	20	-	ns
t <sub>SLS</sub>	t <sub>cyc</sub> /2	-	-	ns
t <sub>CMOD</sub>	-4	0	11	ns
t <sub>MIS</sub>	-	-	7	ns
t <sub>MIH</sub>	3	-	-	ns
t <sub>SHMZ</sub>	-	-	200	ns

### 3.5 I2C Timing

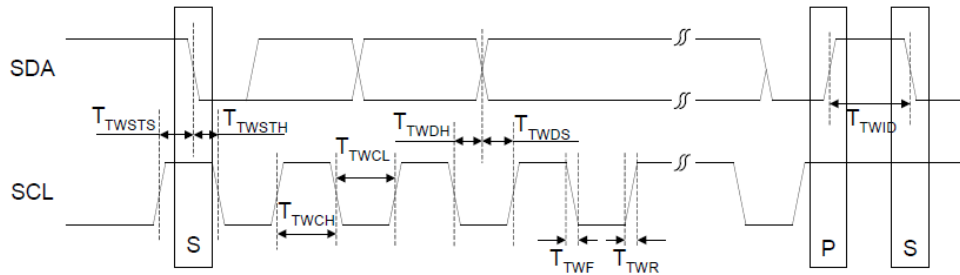


Figure 6 I2C Timing

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	Fscl		100	kHz
Bus Free Time Between Transmissions	TTWID	4.7		us
Start Condition Hold Time	TTWSTH	4.0		us
Clock Low time	TTWCL	4.0		us
Clock High Time	TTWCH	4.0		us
Setup Time for Repeated Start Condition	TTWSTS	4.7		us
SDA Hold Time from SCL Falling	TTWDH	0.1		us
SDA Setup time to SCL Rising	TTWDS	100		ns
Rise Time of SCL	TTWR		25	us
Fall Time SCL	TTWF		25	ns

### 3.6 Reset and Power-on Timing

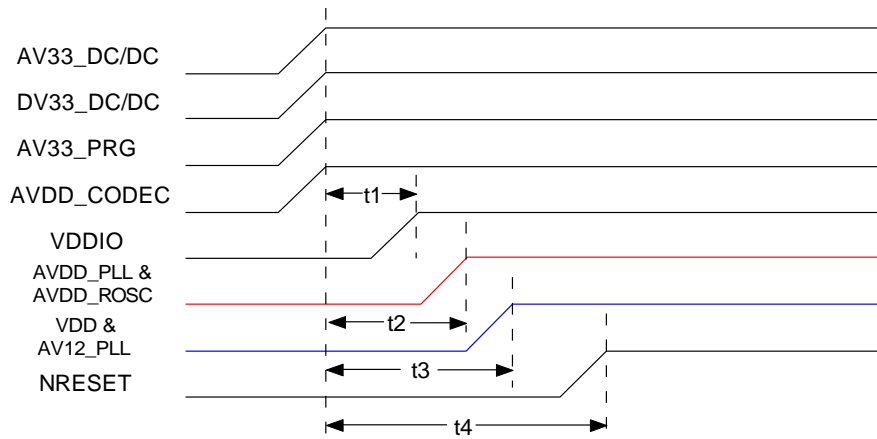


Figure 7 SCT3288 Reset and Power-on Timing

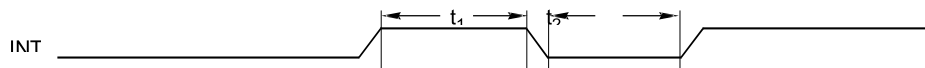
Note:

1. AVDD\_PLL and AVDD\_ROSC in red line derives from AV33\_PRG by on-chip LDO.
2. VDD and AV12\_PLL in blue line derives from AV33\_DC/DC and DV33\_DC/DC by on-chip DC/DC.
3. NRESET should be released after VDD and AV12\_PLL is powered up.

Reference	Description	Min	Max	Unit
t1	Valid DSP to Valid I/O	0		us
t2	On-chip LDO startup time		280	us
t3	On-chip DC/DC startup time		750	us
t4	NRESET release time	1.5		ms

### 3.7 Interrupt Timing

External interrupts INT0 and NMI are edge-triggered and asynchronous. A sampled LOW-to-HIGH transition constitutes a valid interrupt. Figure 8 shows external interrupt timing relative to the processor clock. The table below describes the timing relationships in Figure 8.



**Figure 8 Interrupt Timing**

Reference	Description	Min	Max	Unit
t1	Interrupt HIGH Pulse Width	1	—	T
t2	Interrupt LOW Pulse Width	1	—	T

Note: T = processor clock period.

#### 4 Pin and Signal List

Pin No	Pin Name	Pin Type	Pin Description
1	DEMOD_IN	AI	Demod input
2	RINP	AI	Right ADC differential input positive
3	RINN	AI	Right ADC differential input negative
4	LINN	AI	Left ADC differential input negative
5	LINP	AI	Left ADC differential input positive
6	MIC_IN	AI	Microphone input
7	BEEP_IN	AI	Beep tone input
8	VREFH	P	Codec analog reference positive
9	AVDD_CODEC	P	Codec analog power supply
10	AVSS_CODEC	P	Codec analog ground
11	VREFL	P	Codec analog reference negative
12	ROUT1	AO	Right DAC line output 1
13	ROUT2	AO	Right DAC line output 2
14	VMID	P	Mid-rail reference decoupling point
15	LOUT2	AO	Left DAC line output 2
16	LOUT1	AO	Left DAC line output 1
17	AV33_PRG	P	On chip LDO input, 3.3V typical
18	VOUT_PRG	P	On chip LDO output, 3.0V typical
19	AVSS_PRG	P	Analog ground of LDO
20	DV33_DC/DC	P	On chip DC/DC analog power supply
21	DVSS_DC/DC	P	On chip DC/DC analog ground
22	VOUT_FB	P	On chip DC/DC Output Voltage Feedback Pin
23	AV33_DC/DC	P	On chip DC/DC power input
24	LX_DC/DC	P	On chip DC/DC Output Switch Node
25	AVSS_DC/DC	P	On chip DC/DC power ground
26	VDD	P	Core power supply
27	VDDIO	P	IO power supply
28	NC	-	No connection
29	NC	-	No connection
30	NC	-	No connection
31	NC	-	No connection
32	NC	-	No connection
33	VDD	P	Core power supply
34	I2S_BCLK	I/O	I2S bit clock Slave: input Master: output
35	I2S_LRCK	I/O	I2S frame clock Slave: input Master: output
36	I2S_MCLK	O	I2S main clock Slave: No use Master: output
37	I2S_DI	I	I2S serial data input
38	I2S_DO	O	I2S serial data output
39	VDDIO	P	IO power supply
40	I2C_SCL	O	I2C serial clock output
41	I2C_SDA	I/O	I2C serial data output and input
42	I2S_R_BCLK	I/O	I2S RX bit clock Slave: input Master: output
43	I2S_R_DI	I	I2S RX serial data input
44	TEST	I	Connect to ground
45	VDD	P	Core power supply
46	I2S_R_LRCK	I/O	I2S RX frame clock Slave: input Master: output



47	I2S_T_DO	O	I2S TX serial data output
48	I2S_T_BCLK	I/O	I2S TX bit clock Slave: input Master: output
49	I2S_T_LRCK	I/O	I2S TX frame clock Slave: input Master: output
50	VDDIO	P	IO power supply
51	SPI_MOSI	O	SPI master MOSI
52	SPI_SCLK	O	SPI master serial clock output
53	SPI_MISO	I	SPI master MISO
54	VDDIO	P	IO power supply
55	VDD	P	Core power supply
56	SPI_CSNO	O	SPI master chip select 0 output
57	SPI_CSN1	O	SPI master chip select 1 output
58	SPI_S_CSN	I	SPI slave chip select input from host processor
59	SPI_S_MOSI	I	SPI slave MOSI
60	SPI_S_MISO	O	SPI slave MISO
61	SPI_S_SCLK	I	SPI slave clock input from host processor
62	VDDIO	P	IO power supply
63	HOBIB	O	SPI slave data output status
64	INT0	I	External Hardware Interrupt
65	NMI	I	Non-maskable Interrupt
66	NRESET	I	Chip hardware reset
67	AVDD_ROSC	P	ROSC analog power supply
68	AVSS_ROSC	P	ROSC analog ground
69	AVDD_PLL	P	PLL analog power supply
70	AVSS_PLL	P	PLL analog ground
71	AV12_PLL	P	PLL 1.2V power supply
72	XIN	AI	XIN or external clock generator input
73	XOUT	AO	XOUT
74	VDDIO_OSC	P	IO power supply for internal oscillator
75	VDDIO	P	IO power supply
76	GPIO0	I/O	Programable IO0 (See note is section 5.1.1)
77	VDD	P	Core power supply
78	GPIO1	I/O	Programable IO1
79	GPIO2	I/O	Programable IO2, please see section 6.5 for more details
80	GPIO3	I/O	Programable IO3, please see section 6.5 for more details
81	GPIO4	I/O	Programable IO4, please see section 6.5 for more details
82	GPIO5	I/O	Programable IO5, please see section 6.5 for more details
83	GPIO6	I/O	Programable IO6 (See section 5.1.8)
84	GPIO7	I/O	Programable IO7 (See section 5.1.8)
85	UART_TXD	O	UART transmit
86	UART_RXD	I	UART receive
87	NC	-	No connection
88	MICBIAS	AO	Codec Microphone bias output
epad	VSSD	P	Digital ground

## Note:

1. AO = analog output
2. AI = analog input
3. I/O = bidirectional
4. I = digital input
5. O = digital output
6. P = power or ground

## 5 Component and PCB Recommendations

### 5.1 Recommended External Components

#### 5.1.1 Xtal Interface

The clock circuit can operate with either a Xtal or external frequency oscillator. If using a Xtal, its frequency range should be 12.8 MHz to 26 MHz. If using an external frequency oscillator, its frequency range should be from 12.8 MHz to 40 MHz. Please refer to section 6.1.1 for more details about source clock. Figure 9 shows the different application for Xtal and external frequency oscillator.

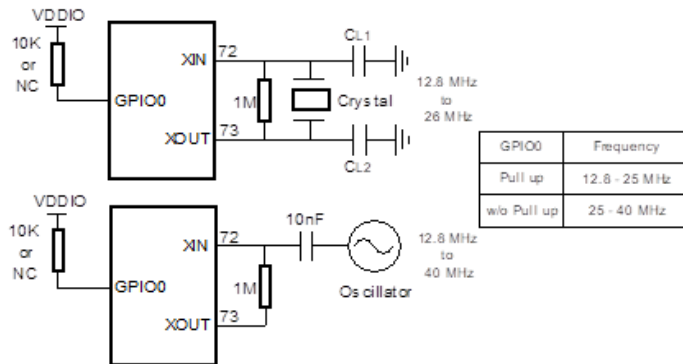


Figure 9 Xtal Interface

**Notes:**

If the operating frequency is between 12.8 MHz to 25 MHz, the GPIO0 must be pulled high by an external 10k resistor or the host processor during reset or power up. For other operating frequencies, GPIO0 should be pulled low or left floating during reset or power up. After the reset or power up, GPIO0 can be used as a normal programmable I/O.

$C_{L1}$  and  $C_{L2}$  are the load capacitances. It is the effective load capacitance for which the crystal is tuned. In the above oscillator circuit, the load capacitance can be calculated by  $C_{L1} * C_{L2} / (C_{L1} + C_{L2})$ . This value can be found in the crystal manufacturer’s user manual. The recommended value is 12 pF.

The tracks between the Xtal and the device pins should be as short as possible to achieve maximum stability and best start up performance. It is also important to achieve a low impedance connection between the Xtal capacitors and the ground plane.

#### 5.1.2 I2C Interface

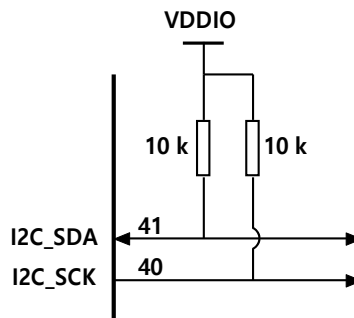


Figure 10 I2C Interface

**Note:**

10 k pull up resistors are necessary if the I2C is used.

### 5.1.3 DC/DC Components

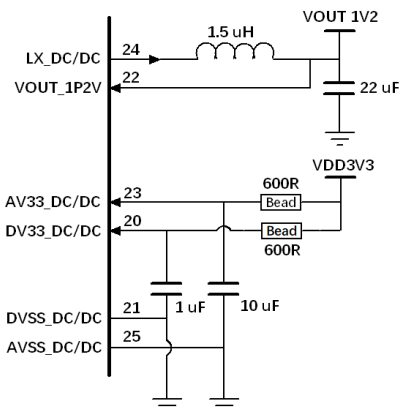


Figure 11 DC/DC Components

#### Notes:

The inductor value affects its peak-to-peak ripple current, the output voltage ripple and the efficiency. For SCT3288 internal DC/DC, a 1.5 $\mu$ H inductor with DCR smaller than 30m $\Omega$  and ISAT larger than 600mA is recommended.

The COUT will influence the output voltage ripple, load response, and the system stability. A 22 $\mu$ F with low-ESR capacitor such as ceramic, it is recommended for COUT. The ESR of COUT shall NOT be larger than 10m $\Omega$ . The COUT should be connected to the inductor as close as possible. Connect the GND side of the capacitors directly to the ground plane of the board.

To prevent large voltage transients, a 10 $\mu$ F low-ESR input capacitor CPIN is required to be placed between AV33\_DC/DC and AVSS\_DC/DC, and a 1.0 $\mu$ F low-ESR input capacitor CAIN is also required to be placed between DV33\_DC/DC and DVSS\_DC/DC. All the capacitors should be placed next to the corresponding pins as close as possible. Connect the GND side of all the capacitors directly to the ground plane of the board.

The input supply trace to its decoupling capacitors should be as short as possible. The decoupling capacitors provide the AC current to the internal power MOSFET and its driver. It is important to minimise the parasitic inductance from the capacitors to the chip pins. Minimise the switching power traces connecting LX\_DC/DC to the inductor to reduce radiated EMI and parasitic coupling. Keep sensitive nodes such as feedback pins away from or shielded from the large voltage swings on the switch node. Minimise the length of the connection between the step-down converter inductor and the output capacitor.

### 5.1.4 LDO Components

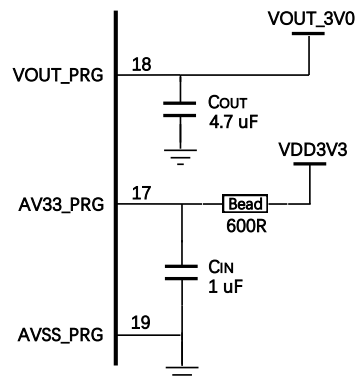


Figure 12 LDO Components

#### Note:

A 4.7 $\mu$ F low-ESR capacitor, like ceramic capacitor, is recommended for COUT. It should be placed next to VOUT\_PRG pin as close as possible.

A 1 $\mu$ F low-ESR capacitor CIN is also recommended to place between AV33\_PRG and AVSS\_PRG. It also needs to be placed closely to the AV33\_PRG pin.

5.1.5 PLL and ROSC

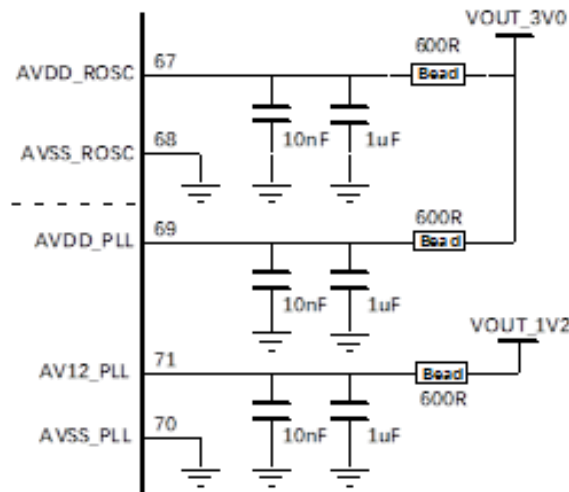


Figure 13 PLL and ROSC Power Supply Decoupling

Note:

VOUT\_3V0 comes from the chip internal LDO output. VOUT\_1V2 comes from internal DC/DC output.

Low-ESR ceramic capacitor 1uF and 10nF should be added between each power pin and ground. As a minimum the 10nF should be placed as close as possible to the power pin. Ferrite bead should be used to separate the analog power domain from digital power domain.

5.1.6 Digital Power and Decoupling

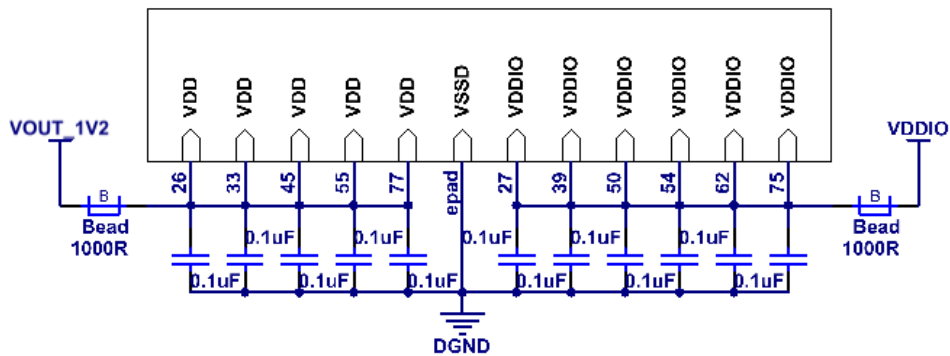


Figure 14 Digital Power and Decoupling

Note:

Core power VDD is supplied from the devices internal DC/DC converter, VDD digital supply pins should be connected to the DC/DC output through a ferrite bead. A decoupling capacitor should be placed for each VDD pin.

VDDIO supplies can be 1.8V to 3.6V and should keep same as the host processor I/O voltage.

A decoupling capacitor should be placed for each VDD pin.

5.1.7 Codec

5.1.7.1 Power and Reference

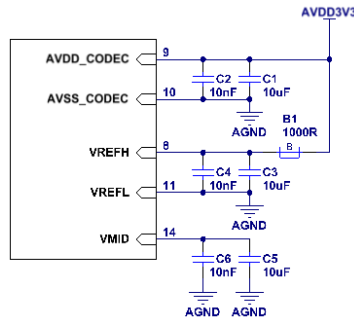


Figure 15 Codec Power and Reference

Note:

Codec should be powered by a dedicated power source to achieve the best performance. The decoupling capacitors should be placed as close as possible to the pins. A ferrite bead is also required to separate analog power from the reference power.

5.1.7.2 Microphone Input

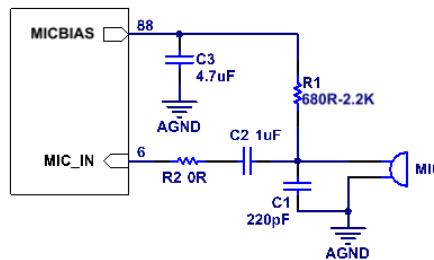


Figure 16 Microphone Input

Note:

The recommended component values are C1=220pF, C2=1uF, R1=680ohm~2.2kohm, R2=0ohm, also refer to the application circuit in the Microphone specification. MICBIAS decoupling capacitor is 4.7uF. The microphone also could be biased by an external power source.

5.1.7.3 Demod and Beep Input

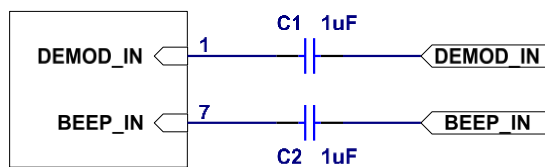


Figure 17 Demod and Beep Input

Note:

The FM demodulated signal should be AC coupled to DEMOD\_IN. 1uF is recommended to achieve the good frequency response and the small transient variable DC.

Beep input also needs a 1uF coupling capacitor.

5.1.7.4 Differential Line Input

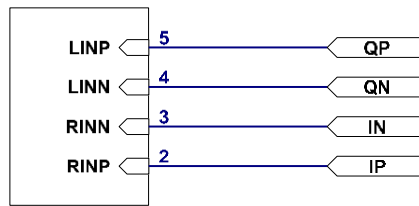


Figure 18 Differential Line Input DC Coupling

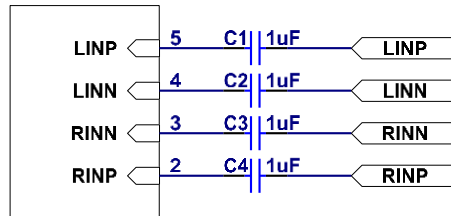


Figure 19 Differential Line Input AC Coupling

Note:

The I/Q signal should be DC coupled to differential line inputs when SCT3288 is used with SCT3811 together. No extra components are required as shown in Figure 18.

It also supports AC coupling, the 1uF coupling capacitor is required as Figure 19.

5.1.7.5 Line Output

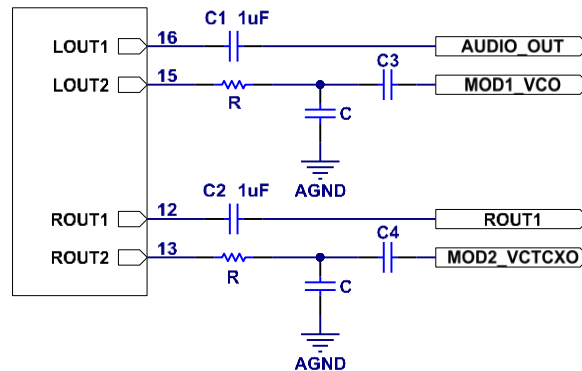


Figure 20 Line Output

Note:

The audio signal is output by LOUT1 and 1uF coupling capacitor is recommended.

The modulation signal is output by LOUT2 and ROUT2. Addition of the RC formed low-pass filter is recommended for both output paths. If two-point modulation is used, it is recommended that LOUT2 is AC coupled to VCO by C3 and ROUT2 should be DC coupled (C4 = 0R) to VCTCXO in order to control the carrier frequency error. ROUT2 could also be AC coupled to VCTCXO, and the carrier frequency error controlled directly by the user, for example use a DAC on the main MCU. The R, C, C3 and C4 value should be determined by design.

5.1.8 GPIO Pins

All GPIO pins are configured as inputs with an internal pull-down circuit by default while the chip powering up. Please note that the GPIO0 needs to be pulled up by 10k resistor if the input clock frequency is lower than 25MHz. Please refer to Figure 9 for more details. After a reset or power up, GPIO0 can be used as a normal programmable I/O.

Please make sure that the GPIO6 has no pull-up resistor and is not pulled high by the host processor while the SCT3288 is resetting or powering up. After the reset or power up, GPIO6 can be used as normal programmable I/O.

## 6 Hardware Description

### 6.1 Clock Generation Unit

#### 6.1.1 Xtal Frequency

The SCT3288 is designed to work with a Xtal, or an external frequency oscillator within the ranges from 12.8 MHz to 40 MHz. If using a Xtal, its frequency range should be 12.8 MHz to 26 MHz. If using an external frequency oscillator, its frequency range can be 12.8 MHz to 40 MHz.

Please make sure the GPIO 0 is pulled up by a resistor when the chip is powering up or resetting if the frequency is between 12.8 MHz to 25 MHz. If the input frequency is between 26 MHz to 40MHz, this pull-up resistor is not needed. Please refer to Figure 9 for more details.

To comply with a DMR/dPMR requirement of 2 ppm on baseband timing, the clock input of SCT3288 should also be within 2 ppm. However, when communicating with another DMR/dPMR terminal also using SCT3288, a maximum tolerance of 20 ppm is acceptable. However, if DMR TDMA direct mode is to be supported, the clock input requirement is 0.5 ppm, per TS 102 361.

A 19.2 MHz or 38.4 MHz TCXO / VCTCXO is strongly recommended as the input clock to achieve the best performance.

#### 6.1.2 PLL

SCT3288 integrates a built-in PLL to generate a high frequency processor clock from a slower off-chip clock source. It supports both integer mode and fraction mode. The highest output frequency can be 200 MHz. The PLL is supplied from an on-chip LDO and DC/DC converter. Please refer to Figure 13 for more details.

The PLL output frequency has been configured to 153.6 MHz (the reference clock can be 19.2 MHz or 38.4 MHz) by default when SCT3288 is booting up, and then SCT3288 will give a response to host MCU when PLL lock is achieved. The PLL will be powered down during the sleep mode and the system clock is switched to ROOSC. All the control procedure is done by SCT3288 automatically according to the system work mode, so no manual intervention is required.

#### 6.1.3 ROOSC

SCT3288 integrates a ring oscillator to generate a 1MHz clock as the default system clock when the chip starts up. It can also be used when the SCT3288 enters sleep mode to maintain some external hardware interrupts, which are used to wake the chip from sleep mode.

The ring oscillator's power supply comes from the on-chip LDO and consumes less than 20uA. Please refer to Figure 13 for more details about the ring oscillator's external components.

### 6.2 Power Supply

#### 6.2.1 DC/DC converter

To maximise power efficiency the SCT3288 has an on-chip low power synchronous step-down DC/DC converter, which converts 1.7 – 3.6V input power to a 1.2V output for the core power supply. Using the DC/DC converter allows the SCT3288 to be operated from a single supply voltage.

The DC/DC converter uses a current-mode, fixed frequency PWM control for optimal stability and transient response, also saving devices. To ensure the high efficiency at light load it will reduce the switching frequency and enter pulse-skip mode automatically. The DC/DC converter provides a maximum current of 300mA. For the DC/DC converter's external components please refer to **Figure 11**. Sharing the DC/DC converter output with other devices is not recommended.

#### 6.2.2 LDO regulator

SCT3288 has an on-chip LDO regulator which provides a suitable power supply for all the analog parts of chip (except the codec which has independent positive and negative supply pins) such as PLL and ROOSC from an external high voltage power supply. It is very convenient for a user to supply the chip with only one voltage although the whole chip needs two kinds of different voltages.

It generates 3V from 3.3V to 3.6V power supply. And it provides a maximum current of 200mA. For its external components please refer to Figure 12.

### 6.2.3 IO Power Supply

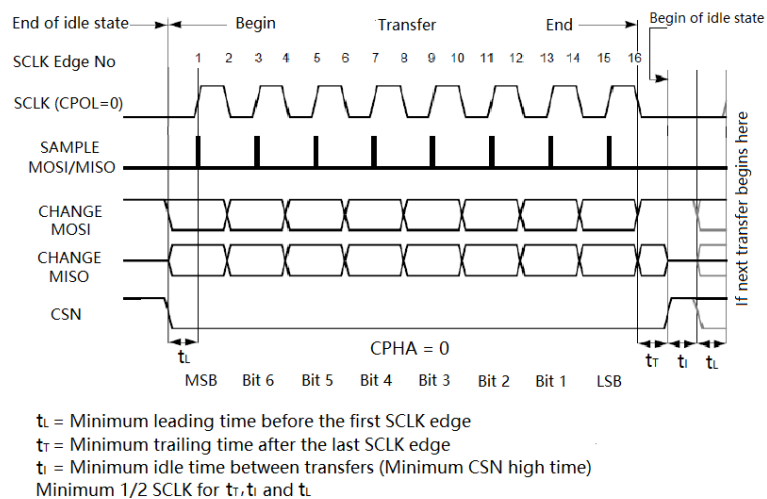
SCT3288 has the dedicated IO power supply VDDIO which can operate from 1.8V to 3.6V. The VDDIO supply should be kept the same as users’ host processor IO voltage. It also could be powered by on-chip LDO if 3.0V is chosen by user as IO voltage.

## 6.3 Serial Interfaces

### 6.3.1 Slave SPI

A slave SPI is used for command, status and data transfers between the SCT3288 and the host processor. All the information has been packaged and defined in a separate document “SCT3288 Packet Interface”. Pin 63 (HOBIB) will go high to notify the host processor when a change in status has occurred or something needs to be reported from the SCT3288 and the processor should read the SCT3288 through the slave SPI and respond accordingly.

MOSI is generated by the master on the falling edge of SCLK and is sampled by the slave (i.e. this SPI interface) on the rising edge of SCLK. MISO is generated by the slave on the falling edge of SCLK. The CSN line must be held low during a data transfer and kept high between transfers. MISO is high impedance when CSN is high. The number of data bytes is dependent on the length of command. The most significant bit is sent first. For detailed timings see section 3.2. This slave SPI operation is shown in Figure 21.



**Figure 21 Slave SPI Operation**

The master SPI has been configured as Table 2 when SCT3288 is booting up from boot ROM. The Data rate is limited to 2Mbps. Please note that this slave SPI works with HOBIB signal together. The HOBIB usually stays low, the host processor should immediately read SCT3288 when the HOBIB goes high, then keep reading until the HOBIB returns to low again.

**Table 1 Slave SPI Default Setting**

Item	Setting
Data Rate	2 Mbps Max
Operation mode	Mode 0, CPOL=0, CPHA=0
MSB or LSB	MSB first
SCLK state	Sample at rising edge, in idle state SCLK is low
Width	16 bits

The default setting of slave SPI is shown as Table 1. This slave SPI interface is compatible with most common processor serial interfaces and may also be easily implemented with general purpose processor I/O pins controlled by a simple software routine.

### 6.3.2 Master SPI

SCT3288 has a master SPI interface. This SPI interface is used for internal functionality while SCT3288 is being powered up or reset and is not available for use during power up and firmware loading.



After the firmware loading, the master SPI interface can be used to control external SPI device such as the SCT3811 and CMX940. The Master SPI interface has two independent chip selector signals for this control purpose. Its main features are as below:

- SPI master is configured with a 32byte FIFO
- Support DMA mode transaction
- Support four SPI operation modes
- Support full duplex operation
- Programmable MSB or LSB

The master SPI has been configured as Table 2 when SCT3288 is booting up from boot ROM. Its operation is the same as slave SPI Interface except it is the master side.

**Table 2 Master SPI Default Settings**

Item	Setting
Data Rate	4M bps
Operation mode	Mode 0, CPOL=0, CPHA=0
MSB or LSB	MSB first
SCLK state	Sample at rising edge, in idle state SCLK is low
Width	8 bits

User can use this master SPI to control an external SPI device by the command of SPI\_OPERATION which is defined in a separate document "SCT3288 packet interface". For example: TBD

**6.3.3 I2C**

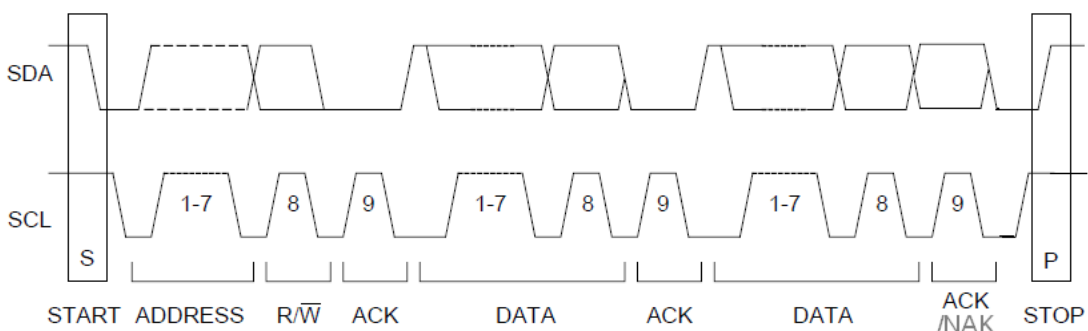
SCT3288 includes one standard I2C master interface to communicate with other external I2C peripherals. The I2C interface can support standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (3.4 Mbps). It supports 7-bit or 10-bit addressing.

The SCT3288 preloaded firmware has configured the I2C as Table 3. Please note that the I2C is disabled by default to save the power consumption.

**Table 3 I2C Default Setting**

Item	Setting
Data rate	Standard mode 100kbps
Address mode	7-bit
Address	by command

I2C interface is a bi-directional serial bus that uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. The timing diagram for data transfer of this interface is given in Figure 22. Data are transmitted synchronously to SCL clock on the SDA line on a byte-by-byte basis. Each bit in a byte is sampled during SCL high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low. The transfer rate of this interface can be 100 kbps.



**Figure 22 Data Transfer for I2C**

SCT3288 as the master initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCL is high.

User can use this I2C to control other external I2C devices by the command of I2C\_OPERATION which is defined in a separate document “SCT3288 packet interface”.

For example: TBD

### 6.3.4 I2S

SCT3288 has three I2S interfaces to transfer data with an external digital audio system or a transceiver with a digital I/Q interface: one operates in full duplex mode, one in Tx only mode and one in Rx only mode.

#### 6.3.4.1 Features

- Master or slave mode of operation
- The data width for each channel is 16 bits, 24 bits or 32 bits
- LRCK pulse width is always 32 times width of BCLK in master mode
- Master side LRCK pulse width should equal or bigger than slave side in slave mode
- Supports audio stereo data or audio mono data transmit and receive
- Supports consecutive or non-consecutive data transmit and receive
- Supports left or right alignment
- Only one channel is needed, and the selection of left or right channel can be configurable when transmit/receive audio mono data
- Serial data is transmitted in two’s complement with the MSB first
- The latch for SD and LRCK can be defined at the rising or falling edge of BCLK
- The format can be switched between delayed (Philips) and non-delayed (non-Philips)
- Interrupt trigger or sentinel available when data in FIFO are empty or full
- The size of embedded FIFO is 32x16 bit, build with internal-register, including TX FIFO and RX FIFO

#### 6.3.4.2 I2S Operation

The I2S interface consists of a Left/Right clock called LRCK which has a frequency equal to the sample rate and is common to both input and output audio signal paths. The LRCK low and high levels indicate if the audio data reflects the left or right channel.

The I2S Interface may be configured to operate as either master or slave. If the SCT3288 I2S is the master, the LRCK, MCLK and BCLK pins are driven by the SCT3288 as outputs. MCLK output frequency must be 256xLRCK. If it is the slave, the LRCK and BCLK pins are configured as inputs and both pins should be driven by the external device. And the MCLK output will be disabled. The I2S Interface transmits serial audio data to the external device on the SDO output pin and receives serial audio data from the external device on the SDI input pin. I2S Interface may be configured to operate in several modes and supports both left and right alignment which are shown in Figure 23 to Figure 26. Please note that it only supports left alignment when it works in slave mode.

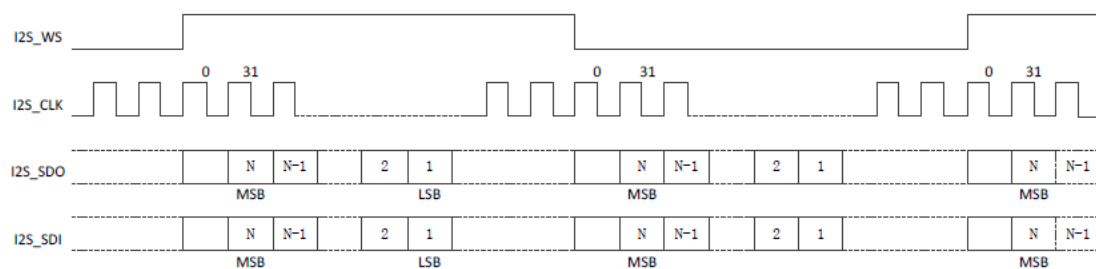


Figure 23 I2S Bus with delay mode, left alignment (N=16, 24, 32)

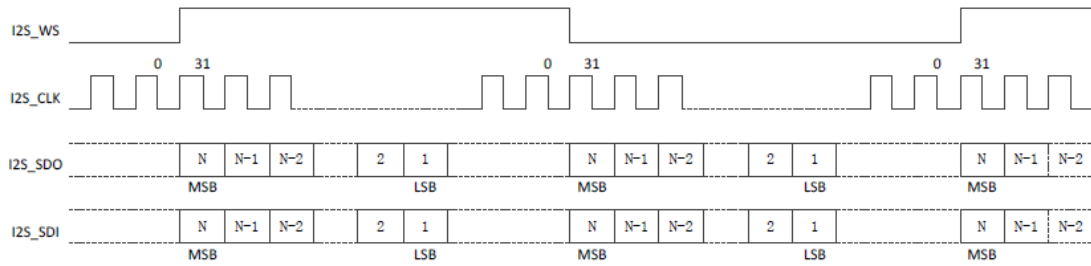


Figure 24 I2S Bus without delay mode, left alignment (N=16, 24, 32)

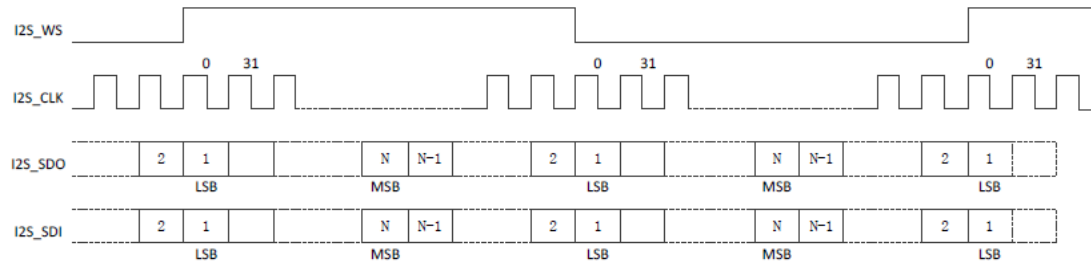


Figure 25 I2S Bus with delay mode, right alignment (N=16, 24, 32)

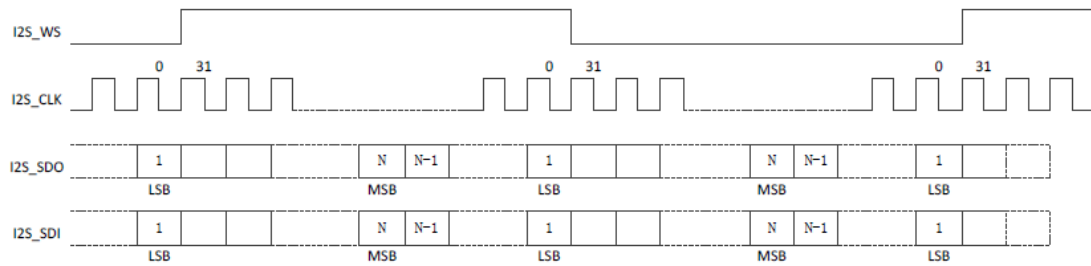


Figure 26 I2S Bus without delay mode, right alignment (N=16, 24, 32)

### 6.3.5 UART

SCT3288 includes a programmable Universal Asynchronous Receiver/Transmitter (UART). The UART can be used to communicate with an external Host. Its main feature are as below:

- Transmit and receive FIFO depths is 16
- Programmable character properties, such as number of data bits per character (5-8), optional parity bit (odd or even) and number of stop bits (1, 1.5 or 2)
- Programmable serial data baud rate

The SCT3288 preloaded firmware has configured the UART as Table 4. Please note that the UART is disabled by default.

Table 4 UART Default Setting

Item	Setting
Data Length	8bits
Stop bit	1 bit
Parity	None
Baud rate	38400

## 6.4 System Interface

This section describes the external system interface signals.

Table 5 System Interface

Signal Name	Input / Output	Descriptions
INT0	Input	External Hardware Interrupts. The INT0 signal provides an external hardware interrupt source to SCT3288. SCT3288 takes an interrupt when INT0 is asserted. INT0 is edge-triggered; a sampled LOW-to-HIGH transition defines one occurrence of the interrupt. INT0 must be asserted for at least one processor clock period to guarantee the interrupt request is taken. INT0 is always sampled on a rising edge of the processor clock, and transitions are ignored during reset. INT0 is used to wake up SCT3288 when it is in SLEEP mode. If unused, INT0 must be tied LOW.
NMI	Input	Non-maskable Interrupt. NMI is an external hardware interrupt that has the highest priority of all the SCT3288 interrupts. NMI is sampled on the rising edge of the processor clock, and must be asserted for a minimum of one processor clock period. A sampled LOW-to-HIGH transition asserts the NMI interrupt request. The processor branches to address 0. NMI has the same effect of a reset, without code downloading from the flash. If unused, this signal must be tied LOW.
NRESET	Input	Device Reset. This signal starts SCT3288 reset process. After the initial power-up sequence, NRESET must be asserted (LOW) for a minimum of five processor clock cycles to guarantee proper reset of the device. The LOW-to-HIGH transition of this signal causes the chip boot up from the internal boot ROM.

## 6.5 Programmable I/O

The SCT3288 provides eight programmable I/O signals, GPIO[7:0], for general-purpose hardware interfacing. Each of these signals can be individually configured as input or output. The memory-mapped PIO register controls the behaviour of these signals.

The SCT3288 preloaded firmware has assigned the GPIO with the following functions:

Table 6 Programmable I/O Signals

GPIO Number	Input / Output	Descriptions
GPIO 0		
GPIO 1		
GPIO 2	output	Slave SPI handshake with host MCU It uses a rising edge to inform the host MCU that SCT3288 has data that needs to be reported. Then HOBIB goes high to indicate that the data is ready.
GPIO 3	output	DMR mode RF Timing port
GPIO 4	output	SCT3811 High/Low injection indication (available on SCT3288xxM only)  Low: Switch to Low injection High: Switch to High injection
GPIO 5	output	SCT3288 work mode indication Low: Normal Mode High: Low Power Mode
GPIO 6		
GPIO 7		

## 6.6 Codec

SCT3288 integrates a codec which has 2-channel 24bit sigma-delta ADC with two single-ended inputs and two differential input pairs and 2-channel 24bit sigma-delta DAC with two pairs line output. The codec also has an audio PLL to support a wide range of sample rates from 8 kHz to 96 kHz.

### 6.6.1 Features

- ADC  
--THDN: -82dB

- Dynamic Range, SNR: 96dB
- DAC Line Output
- THDN: -80dB
- Dynamic Range, SNR: 98dB
- Stereo Line Input and Mono Microphone Input
- Internal 24-Bit Fractional PLL as the Audio CODEC Master Clock Generator
- Sampling Rates 8 kHz to 96 kHz
- Input overflow detection
- Stereo/Mono Mode
- Power Supply
- Digital Core: 1.2V
- Analog: 2.25V ~ 3.6V, 3.3V typical

## 6.6.2 Codec Block Diagram

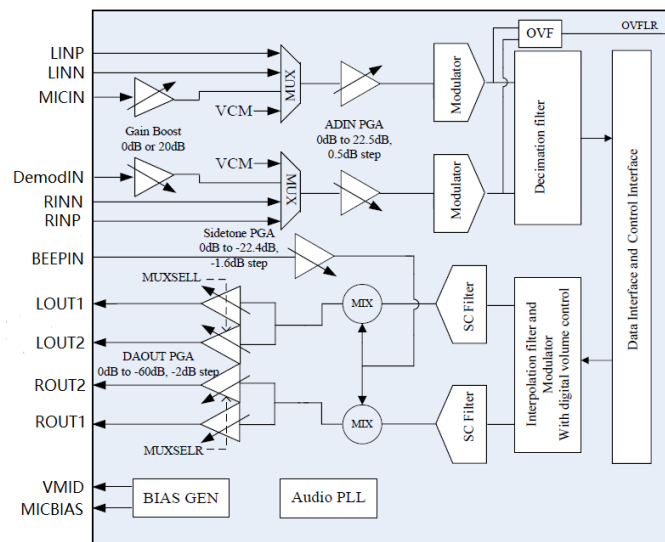


Figure 27 Codec Block Diagram

## 6.6.3 Codec Description

### 6.6.3.1 Sigma-Delta ADC/DAC

The codec integrates 2-channel 24-bit sigma-delta ADC and 2-channel 24-bit sigma-delta DAC. Such architecture allows for infinite adjustment of sample rate while maintaining linear phase response simply by changing the master clock frequency.

### 6.6.3.2 Line Inputs

The codec includes six analog inputs pins 2 of which are fully-differential pairs and 1 pair of stereo single-ended inputs. The inputs are separated to left and right channel and connected to two multiplexers. Each multiplexer is followed by a PGA (programmable gain amplifier) which can provide 0 dB to 22.5 dB gain with 0.5 dB step.

The left and right channel differential line-in inputs are high impedance, low capacitance. There is no internal AC coupling capacitance inside the codec. Each channel includes independent PGA and mute function. Passive RF and active Anti-Alias filters which has a  $f_c$  near 510KHz are also incorporated within the line inputs to prevent high frequencies aliasing into the audio band or otherwise degrading performance. The inputs PGA are biased internally through the operational amplifier to VMID. DC coupling for ADC analog signal is supported which is shown in Figure 18. It is recommended to maintain input signal common mode voltage near VMID for better performance. The recommended common mode voltage value will be  $AVDD/2$ , for better swing of internal circuit and preventing clipping at PGA output. The AC coupling is also supported, the external components required are shown in Figure 19. Please refer to Figure 30 and Figure 36 for the typical application about these analog signal path.

The Codec provides 2 single-ended inputs which are MIC\_IN and DEMOD\_IN. An extra gain boost is inserted for MIC\_IN and DEMOD\_IN path between the inputs and multiplexer. This gain boost provides 0 dB or 20 dB gain. Please refer to Figure 28 and Figure 29 for typical application about these analog signal path.

The codec also has a BEEP\_IN which is looped to line out directly through a PGA and a mixer. It is used to loop a user defined tone which is generated by host processor to audio signal output or modulation signal output.

The external components required are shown as Figure 16 and Figure 17.

#### **6.6.3.3 Line Outputs**

The Codec provides four low impedance line outputs, suitable for driving typical line loads of impedance 10k and capacitance 50pF. Each output has an independent PGA and can be controlled independently. Please refer to Figure 28 and Figure 29 for typical application about these analog signal paths. The external components required are shown in Figure 20.

#### **6.6.3.4 PLL**

The Codec's operating master clock is 256 fs, and it supports a wide range of sample rates (fs) from 8 kHz to 96 kHz just simply by changing the operating master clock. The PLL here is used to produce the master clock from the input reference clock. The output of the PLL is 256 fs.

#### **6.6.3.5 ADC Input Overflow Detection**

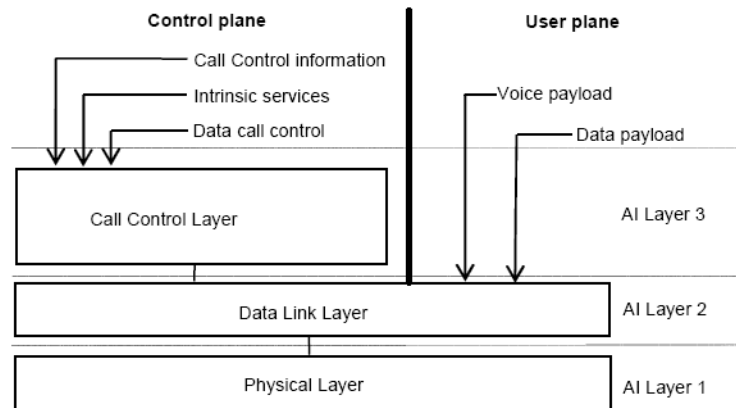
This Codec supports input overflow detection. An averaging filter is used for each ADC modulator output bitstream. This filter supports a selectable window width and programmable overflow threshold. If the filter output of a channel exceeds the pre-defined threshold value (either positive or negative) at any time, then associated flag signal OVFLR will be pulled up to logic "1", which indicates input is overflow.

This function is very useful to avoid the RF front-end being saturated by an out band strong signal.

## 7 Detailed Description

### 7.1 dPMR and DMR Implementation

SCT3288 supports the physical layer (layer 1), data link layer (layer 2), and call control layer (layer 3) of dPMR and DMR. Annex A of TS 102 490 / TS 102 658 and Annex C of TS 102 361-2 are also implemented. The user is expected to develop the application layer on the external MCU. This is illustrated in the diagram below.



More specifically, the following are implemented in SCT3288 for each of the air interface layer.

#### Air Interface Physical Layer (Layer 1)

1. 4FSK modulation and demodulation, with programmable modulation index
2. Bit and Symbol definition
3. Frequency and symbol synchronization
4. Transmission burst building and splitting
5. BER test mode complied with O.153

#### Air Interface Data Link Layer (Layer 2)

1. Channel coding (FEC, CRC)
2. Interleaving, de-interleaving and bit ordering
3. Framing, super frame building and synchronization
4. Burst and parameter definition
5. Link addressing (source and destination)
6. Interfacing of voice applications (vocoder data) with PL
7. Data bearer services
8. Exchange signalling and user data with the CCL

#### Air Interface Call Control Layer (Layer 3)

1. Establishing, maintaining and termination of calls
2. Individual or group call transmission and receptions
3. Destination addressing
4. Automatic matching of Called ID of incoming call to own ID and group ID
5. Late entry call support

#### dPMR CSF (Annex A) Support

1. Full support of Standard User Interface (defined in Annex A of TS 102 490/TS 102 658)
2. Allows wild character dialling with "\*"
3. Allows abbreviated dialling
4. Allows mask dialling
5. Syntax checking of dialled digits

## DMR Dialling Number (Annex C) Support

1. Support of dialling number plan (defined in Annex C of TS 102 361-2)
2. Allows group calls with wild character “\*”
3. Syntax checking of dialled digits

## 7.1.1 Signal Flow for DMR/dPMR Transmitter

The signal flow of the DMR/dPMR transmitter is shown in the diagram below.

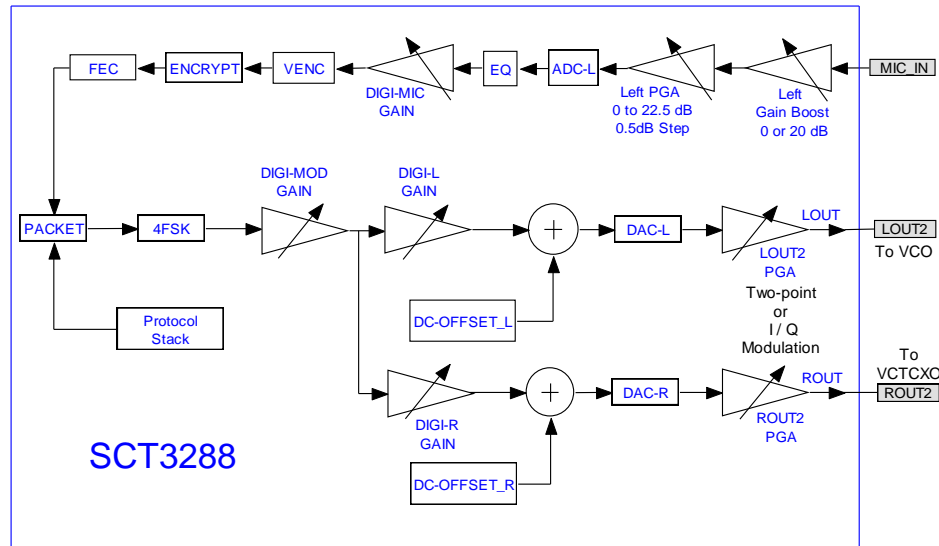


Figure 28 Signal Flow for DMR/dPMR Transmitter

The microphone signal is input from MIC\_IN and amplified by the gain boost and the left PGA, then converted into digital form by the left ADC and stored in the left input channel buffer of SCT3288. The following steps are applied to the digitized signals:

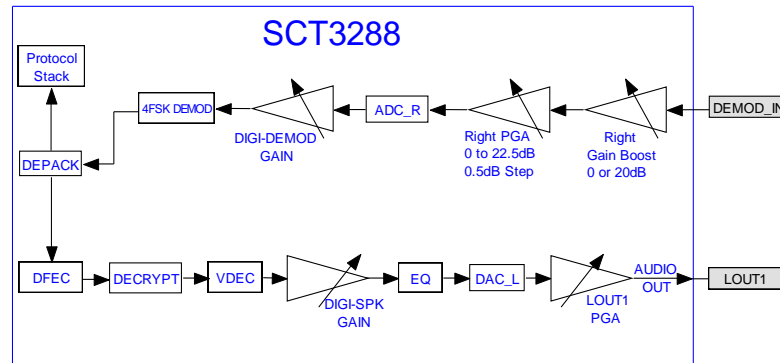
1. 3-stage equalizer.
2. Digital microphone gain, which provides a digital gain to the microphone. It is usually an attenuation to prevent microphone being saturated and to ensure that the signal level is at the optimum level to ensure best voice encoder performance.
3. VENC, the voice encoder, which compresses the voice signals into a 2400 bps encoded signals
4. ENCRYPT, optional encryption block with configurable key
5. FEC, channel coding block, which adds an additional 1200 bps of error correction to the encoded voice signal to form a 3600 bps signals with protection for bit error
6. PACKET, which adds header and control information to form 4800 bps signals
7. 4FSK modulator
8. DIGI\_MOD\_GAIN, a gain block with linear 16-bit gain, for adjusting the modulation index

The resulting signals are split into left channel and right channel signals for two-point modulation or I/Q modulation. Independent DC offsets and analog and digital gains are applied to the left and the right channels. The left channel control and the right channel control are identical, except that the left channel is multiplexed as speaker output in the RX mode. If DC coupling is used, the right channel ROUT2 is to be connected to VCTCXO input, while the left channel LOUT2 is connected to VCO. If AC coupling is used for VCTCXO control, either left or right channel can be connected to TCXO or VCO.



### 7.1.2 Signal Flow for DMR/dPMR Receiver

The signal flow of the DMR/dPMR receiver is shown in the diagram below.

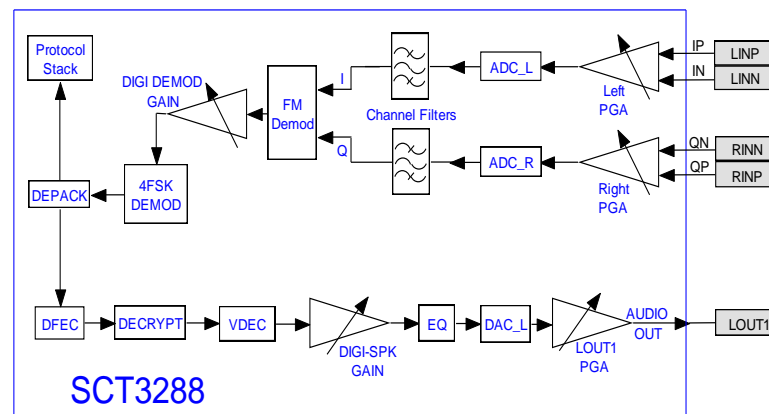


**Figure 29 Signal Flow for DMR/dPMR for FM Demodulated Signal Input**

The FM demodulated signal is input from DEMOD\_IN and amplified by the gain boost and the right PGA, then converted into digital form by the right ADC and stored in the right input channel buffer of SCT3288. The following steps are applied to the digitized signals:

1. DIGI\_DEMOD\_GAIN, a gain block with linear 16-bit gain
2. 4FSK demodulator
3. DEPACK, which removes header and extracts control and voice information
4. DFEC, channel decoding block, which recovers the encoded voice bits and corrects for bit errors
5. DECRYPT, the optional decryption block with configurable key
6. VDEC, the voice decoder, which reconstructs voice signals
7. Digital Speaker Gain
8. 3-stage equalizer

The reconstructed voice signals are converted into analog form by the left DAC and then amplified by LOUT1 PGA before feeding to the audio PA.



**Figure 30 Signal Flow for DMR/dPMR Receiver for I/Q Signal Input**

For the I/Q signal case shown as Figure 30, the differential analog I/Q signals are input to the codec directly. Additional processing is performed, such as channel selection filtering and FM demodulation but the remaining digital processing is the same as in the demodulated case.

For digital I/Q signals, these can be input through the I2S interface directly. And further digital processing is same as the analog I/Q case.

### 7.1.3 RF Timing Control for DMR

The DMR signal is a two time slot TDMA signal, each slot occupying 30 milliseconds. In the RX mode, SCT3288 acquires timing from the synchronization pattern of the far end base station or mobile station. SCT3288 has an internal Slot Timing Signal (as shown in Figure 31) that is aligned with the FM demodulated signals or the I/Q signals at the input. In the TX

mode, SCT3288 controls the timing of the 4FSK modulation signals so that they are aligned with this internal RF timing signal. At the same time, an external signal is derived from the Slot Timing Signal and output through the RF\_TIMING port to control the opening of the RF circuit and PA. The RF\_TIMING signal is a square wave signals, with a period of 60 milliseconds. The RF\_TIMING signal can be exactly the same as the internal Slot Timing Signal, or offset from the Slot Timing Signal through MCU programming. The high level of RF\_TIMING signal corresponds to RF circuit on, while the low level corresponds to RF circuit off. The MCU can derive the timing control signal to drive the RF transceiver or PA through the RF\_TIMING signal from SCT3288.

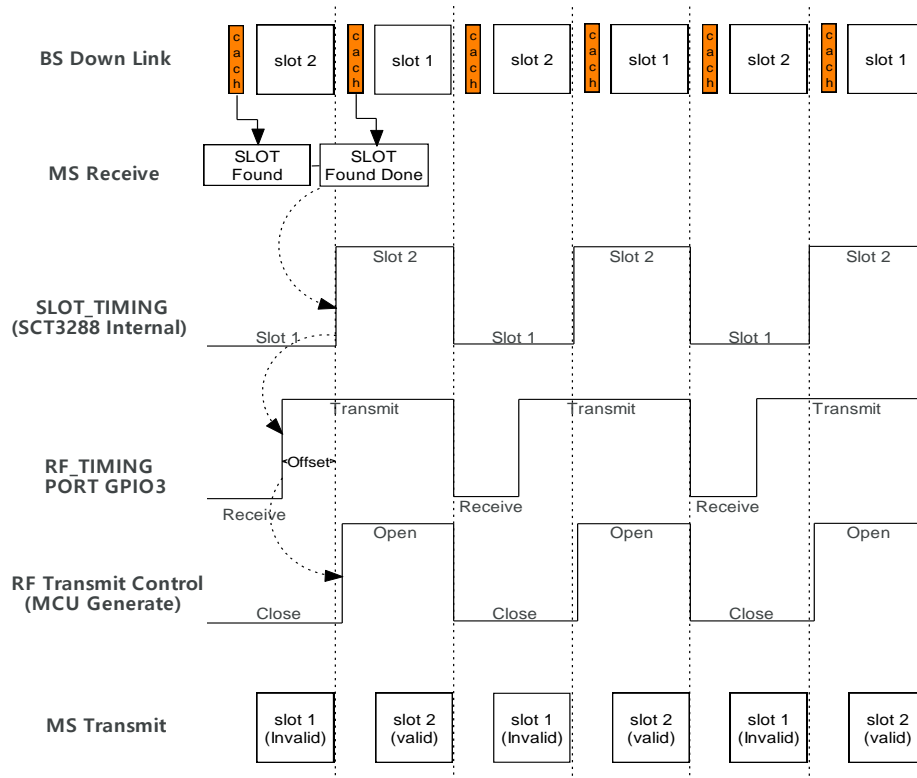


Figure 31 TDMA Timing Control

7.1.4 Vocoder Support

SCT3288 supports the following vocoder:

- Build-in AMBE+2™<sup>1</sup> vocoder from DVSI
- Support 1031 Hz Tone and Silence Test Mode

7.2 Analog Radio Support

The SCT3288 supports tri-mode operation with dPMR, DMR and analog radio. For analog radio, the device complies with related standards for analog radio including TIA 603D and ETSI EN-300296.

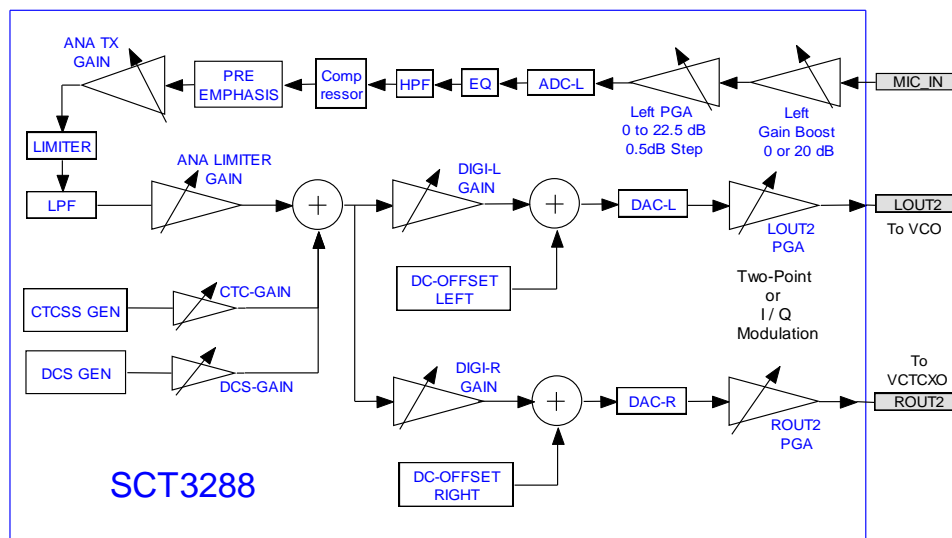
SCT3288 analog processing blocks include:

<sup>1</sup> The AMBE+2™ voice coding technology embodied in this product is protected by intellectual property rights including patent rights, copyrights and trade secrets of Digital Voice Systems Inc. This voice coding Technology is licensed solely for use within this communications equipment. The user of this Technology is explicitly prohibited from attempting to extract, remove, decompile, reverse engineer or disassemble the object code, or in any other way convert the Object Code into human readable form. US Patent numbers #8,595,002, #8,433,562, #8,359,157, #8, #8,200.497, #8,036,886 and #6,912,495B2

- HPF, with stop band at 255 Hz and pass band at 300 Hz
- LPF, with pass band at 2550 Hz or 3000 Hz, and stop band at 6000 Hz
- Componder
- Pre-emphasis filter and de-emphasis filter at 6 dB/octave
- Limiter to limit the maximum frequency deviation
- Sub audio filter with pass band at 255 Hz and stop band at 300 Hz
- CTCSS/DCS generation and detection supporting 38/51 CTCSS code and 83/107 DCS code
- Support for blind CTCSS/DCS detection
- Support for automatic polarity detection for DCS code
- Support for arbitrary CTCSS/DCS code
- 3-stage equalizer

### 7.2.1 Signal Flow for Analog Transmitter

The signal flow of the analog transmitter is shown in the diagram below.



**Figure 32 Signal Flow for Analog Transmitter**

The microphone signals are input from the MIC\_IN pin and amplified by the gain boost and the left PGA, then converted into digital form by the left ADC and stored in the left input channel buffer of SCT3288. The following steps are applied to the digitized analog signals:

1. 3-stage equalizer.
2. HPF, with pass band at 300 Hz, and stop band of 255 Hz.
3. Compressor.
4. Pre-emphasis filter, with 6 dB/Octave.
5. ANA\_TX\_GAIN, a gain block with linear 16-bit gain
6. Limiter for limiting the frequency deviation for large signals.
7. LPF, with selectable corner of 2.55 kHz or 3kHz.
8. ANA\_MOD\_GAIN, a gain block with 16-bit gain after the limiter.

Beside the gain blocks, analog features that can be configured in the transmitter include:

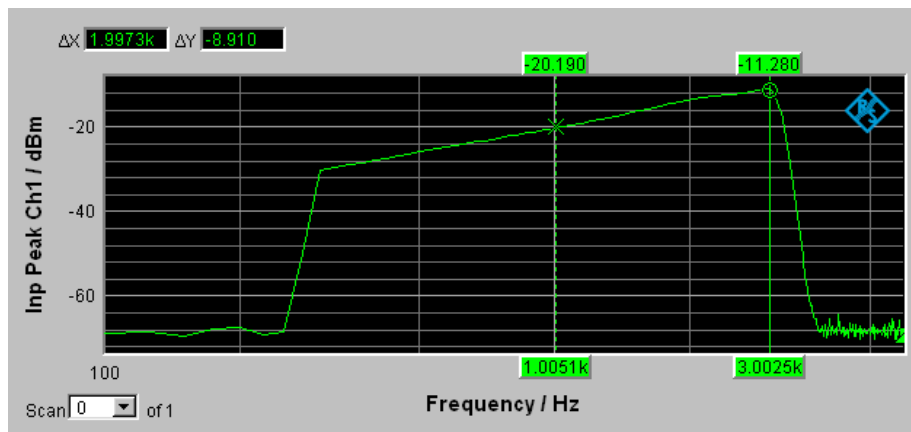
1. BYPASS\_FILTER: when enabled, all analog filters are by passed. A flat frequency response from 0-12 kHz results.
2. BYPASS\_EMP: when enabled, pre-emphasis filter is by passed. A flat frequency response from 300 Hz to 2.55/3 kHz results.
3. CH\_SEL: when enabled, the low pass corner is 3 kHz; when disabled, the low pass corner is 2.55 kHz.

The following table shows the composite frequency responses of channel filters based for different settings of BYPASS\_FILTER, BYPASS\_EMP and CH\_SEL.

**Table 7 Frequency Response of the Analog Transmitter**

Frequencies (Hz)	BYPASS_ FILTER = 1 (in dB)	BYPASS_FILTER = 0 (in dB)			
		BYPASS_EMP = 0		BYPASS_EMP = 1	
		CH_SEL = 0	CH_SEL = 1	CH_SEL = 0	CH_SEL = 1
100	0.0	-49.6	-48.6	-46.3	-46.8
250	0.0	-49.6	-47.6	-49.3	-50.3
300	0.0	-10.0	-9.9	0.5	0.5
350	0.0	-8.8	-8.6	0.5	0.5
500	0.0	-5.6	-5.6	0.4	0.4
700	0.0	-2.9	-2.9	0.2	0.2
1000	0.0	0.0	0.0	0.0	0.0
1500	0.0	3.8	3.7	0.3	0.2
2000	-0.1	6.2	6.4	0.3	0.5
2500	0.0	8.1	8.0	0.4	0.2
3000	-0.1	-12.0	9.3	-21.2	0.0
3500	-0.1	-46.1	-21.4	-49.3	-31.3
6000	-0.2	-50.6	-47.6	-50.3	-49.3

An example of the frequency response is also shown in Figure 33.

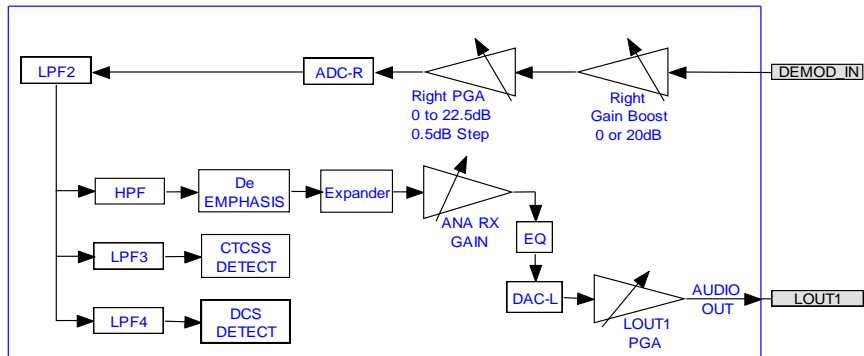


**Figure 33 Frequency Response of the Transmitter with CH\_SEL=0, BYPASS\_EMP = 0, BYPASS\_FILTER = 0**

If CTCSS/DCS is enabled, the internally generated CTCSS/DCS signals are added to the voice signals. The amplitude of the CTCSS/DCS can be modified by CTC\_GAIN or DCS\_GAIN block.

The resulting signals are split into left channel and right channel signals for two-point modulation or I/Q modulation. Independent DC offsets and analog and digital gains are applied to the left and the right channels. The left channel control and the right channel control are identical, except that the left channel is multiplexed as speaker output in the RX mode. If DC coupling is used for TCXO control, the right channel ROUT2 is to be connected to VCTCXO input, while the left channel LOUT2 is connected to VCO. If AC coupling is used for VCTCXO control, either left or right channel can be connected to TCXO or VCO.

## 7.2.2 Signal Flow for Analog Receiver



### SCT3288

**Figure 34 Signal Flow for Analog Receiver with FM Demodulated Signal Input**

The signal flow of the analog receiver is shown as Figure 34. The FM demodulated signal is input from the DEMOD\_IN pin and amplified by the gain boost and the right PGA, then converted into digital form by the right ADC and stored in the right input channel buffer of SCT3288. The following steps are applied to the digitized analog signals:

1. LPF2, with low pass corner at 3000 Hz.
2. HPF, with pass band at 300 Hz, and stop band of 255 Hz.
3. De-emphasis filter, with 6 dB/Octave.
4. Expander.
5. ANA\_RX\_GAIN, linear 16-bit gain.
6. 3-stage equalizer.

The filtered digital signals are converted into analog form by the left DAC and then amplified by the LOUT1 PGA before feeding to the audio PA.

Beside the gain blocks, analog features that can be configured in the receiver include:

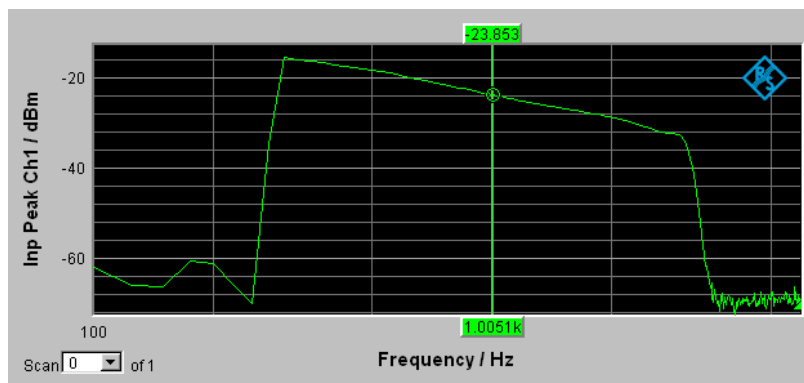
1. BYPASS\_FILTER: when enabled, all analog filters are by passed. A flat frequency response from 0-12 kHz results.
2. BYPASS\_EMP: when enabled, de-emphasis filter is by passed. A flat frequency response from 300 Hz to 2.55/3 kHz results.

The following table shows the composite frequency responses of channel filters based for different settings of BYPASS\_EMP.

**Table 8 Frequency Response of the Analog Receiver**

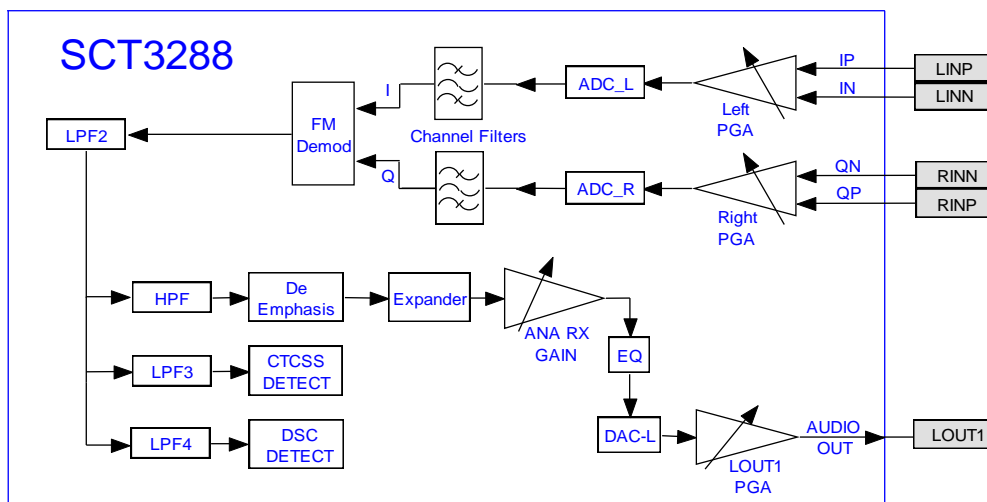
Frequencies (Hz)	BYPASS_FILTER = 1 (in dB)	BYPASS_FILTER = 0 (in dB)	
		BYPASS_EMP = 0	BYPASS_EMP = 1
100	0.0	-39.9	-47.9
250	0.0	-53	-54.3
300	0.0	8.4	0.5
350	0.0	7.6	0.5
500	0.0	5.5	0.4
700	0.0	3.0	0.2
1000	0.0	0.0	0.0
1500	0.0	-3.2	0.2
2000	0.0	-5.4	0.5
2500	-0.1	-7.7	0.2
3000	-0.1	-9.6	0.0
3500	-0.3	-41.6	-31.6
6000	-0.4	-53.5	-54.3

An example of frequency response is also shown in the figure below.



**Figure 35 Frequency Response of the Transmitter with BYPASS\_EMP=0, BYPASS\_FILTER=0**

Two additional low pass filters are applied to the output of LPF2 to extract CTCSS and DCS signals for detection. The detection results are reported to the host processor through slave SPI interface.



**Figure 36 Signal Flow for Analog Receiver with I/Q Signal Input**

For the I/Q signal case shown as Figure 37, the differential analog I/Q signals are input to codec directly. Additional processing is required to be performed, such as channel selection filtering and FM demodulation but the rest of the remaining digital processing is the same as in the demodulated case.

For digital I/Q signals, these can be input through the I2S interface directly. And the other further digital processing is same as the analog I/Q case.

### 7.3 Premium Features (please refer to CML/Sicomm for further information on availability)

Premium features are features specific to SCT3288 but not defined in the dPMR protocol. These won't affect interoperability with other implementation of dPMR protocol and provides useful extensions to the protocol.

#### 7.3.1 Encryption

SCT3288 supports 16-bit scrambler for voice encryption. In addition, for dPMR only mode, the SCT3288 also supports 64-bit DES and 192-bit triple DES. Note that encryption should be managed externally by the host MCU; an external encryption user guide is available.

#### 7.3.2 Voice Recording and Play Back

The SCT3288 is capable of providing support for voice recording and play back. When enabled, the encoded voice bit stream can be passed to the MCU for saving to memory (internal to the MCU or external for longer durations of recording). Due to the high compression ratio of the vocoder, large quantity of speech can be saved efficiently to small size memory. In particular, 40 minutes of speech can be saved in 1 Mbytes of flash memory.

Local near end and remote far end speech can be saved. Play back can be local or remote as well. Remote play back is especially useful in broadcasting pre-recorded speech contents.

### 7.4 Boot Loading

The SCT3288 is designed to boot up from boot ROM, it initializes the PLL and slave SPI automatically after power up and reset by the host processor. It will then follow the procedure below.

1. HOBIB goes high and the SCT3288 will give a response "84 A9 61 00 02 00 17 0E" to host processor over the slave SPI if the PLL is locked and initialization is successful. The host processor should read this response till the HOBIB signal goes low again.
2. The SCT3288 will keep waiting until the host processor sends the command "74 A9 01 00 01 00" to start boot loading.
3. When boot loading is successful, SCT3288 will give a response "84 A9 61 00 02 00 17 01".

After power up and reset, if host MCU does NOT get the response "84 A9 61 00 02 00 17 0E" from SCT3288 within 1 seconds, boot up has failed: and the user should check the power supply and clock input.

### 7.5 Work Mode

The SCT3288 supports three working modes which are normal mode, sleep mode and halt mode.

Table 9 SCT3288 Work Mode

Work Mode	PLL	ROSC	I/O	Codec	Wake up by	Description
Normal Mode	On	Off	Active	Normal	-	Normal mode
Sleep Mode	Off	On	Stop	All off except Vref	INT0	System clock and peripherals inactive. Any enabled external interrupt (INT0), NMI, or reset wakes device. PLL retains lock.
Halt Mode	Off	On	Stop	All off	NMI	System clock and peripheral is inactive. Only NMI or reset wakes device.

### 7.5.1 Normal Mode

In normal mode, the processor executes at full speed and all peripherals are active.

### 7.5.2 Sleep Mode

In sleep mode, the processor clock and all I/O activity stops. While in sleep mode, memory and register contents remain intact. After an enabled, external interrupt with a priority equal to or above the current system priority (INT0), or NMI occurs and is serviced, execution resumes with the instruction following the Sleep instruction.

The host can set SCT3288 into SLEEP mode by using command **CHIP\_LOW\_PWR**, with Low Power Mode 5. To return to normal mode, the host need to insert an external INT0 interrupt to SCT3288. Details can be found in "SCT3288 Packet Interface".

### 7.5.3 Halt Mode

In halt mode, the processor clock and all I/O activity stops. While halted, memory and register contents remain intact, but previous program execution cannot resume. If an NMI wakes up the device from halt mode, the NMI interrupt service routine is instruction following the Halt instruction.

The host can set SCT3288 into HALT mode by using command **CHIP\_LOW\_PWR**, with Low Power Mode 6. To return to normal mode, the host need to insert an external NMI signal to SCT3288. Details can be found in "SCT3288 Packet Interface".



# 8 Typical Application Circuit

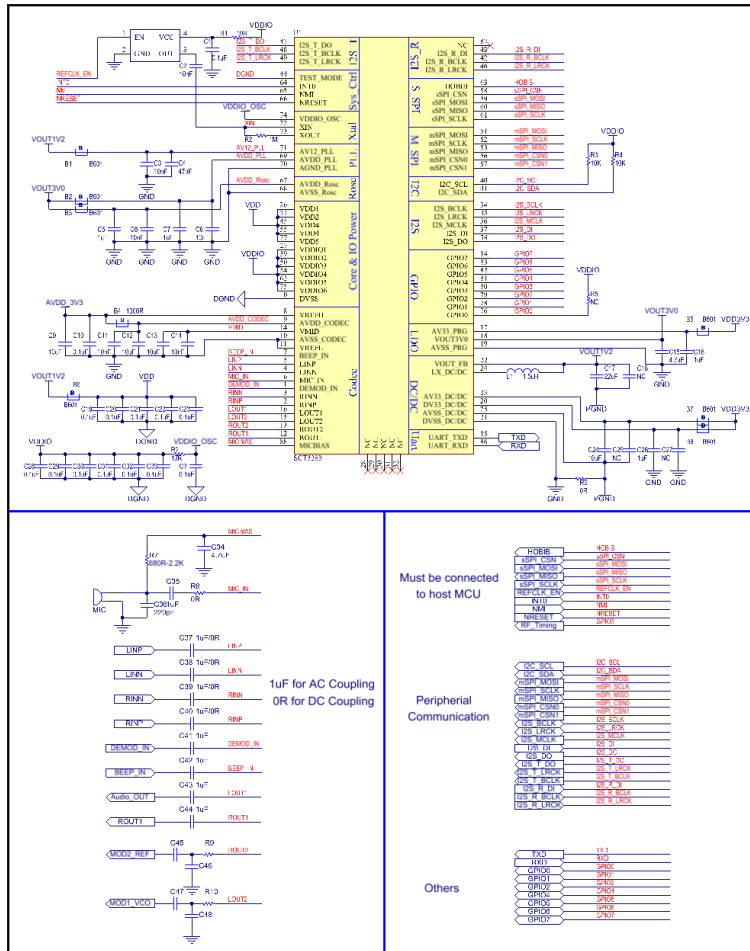


Figure 37: SCT3288 Application Circuit

## 9 Packet Interface

The SCT3288 packet interface is defined for communications between the SCT3288 and the host MCU. The packet format is identical regardless of physical interfaces. Packet details are defined in a separate document: “SCT3288 Packet Interface”.

10 Packaging

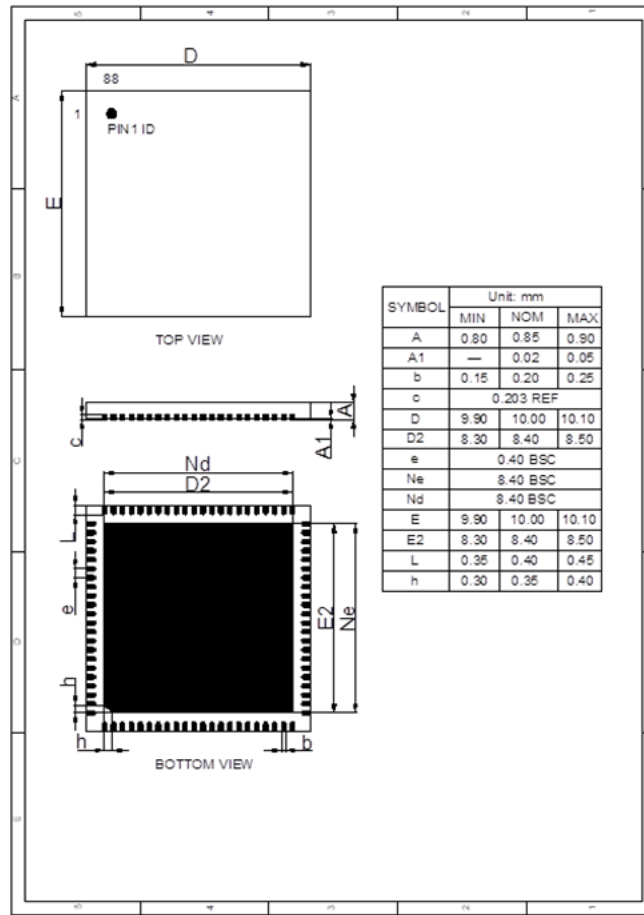


Figure 38 Mechanical Outline of SCT3288 QFN88 Package

## 11 Ordering Information

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Design Support/Package Information page of the CML website: [[www.cmlmicro.com](http://www.cmlmicro.com)].

Order as part no. SCT3288TDM or SCT3288TD

The above product code suffix letters define the following:

T = supported protocols are DMR, dPMR and analog

D = supported vocoder is DVSI AMBE+2

M = supported RF interface is CMX994E or Sicomm SCT3811

SCT3288TD defines similar protocol and vocoder options but with conventional RF support.

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electrostatic discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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