CML Microcircuits

COMMUNICATION SEMICONDUCTORS

Application Note

CMX7031 Synthesiser Lock Time

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1 Introduction

This document has been produced to illustrate the performance of the integrated synthesisers used in the CMX7031 Two-Way Radio Processor IC.

The functionally complete CMX7031 IC includes two fully programmable on-chip synthesisers; both are designed to operate from 100MHz to 600MHz and are both Integer-N types. The advantages of this approach are that it becomes easier to develop closely coupled, low noise and well understood two-way radios with only external VCO and loop filter components required.

This application note must be used in conjunction with the CMX7031 datasheet and user manual. It is intended that this application note can be used with all versions of Function Image™.

2 Evaluation Results

The term "lock" refers to the moment when the synthesiser "locks" to the required frequency and the desired output frequency remains static over time. The CMX7031 includes mechanisms for detecting the lock and reporting it to the host microcontroller via the CMX7031 C-BUS serial interface.

Both synthesisers report their state via an RF Channel Status Register ($B4) via a flag bit that can also be set to drive the IRQN pin (via Interrupt Mask Register $CE). N and R Synthesiser division ratios (of which there are two pairs available for each synthesiser) can be set easily using the RF Channel Data Register ($B2) and lastly controlled by using the RF Channel Control Register ($B3). Details of each of these registers can be found in the CMX7031 user manual.

For the following trace images the PE0201 Evaluation Kit was used; a CMX7031 Function Image™ was used throughout. No modifications were made to the standard PE0201 Evaluation Kit.

It should be noted that the first IRQN following the request to achieve lock does not constitute full lock. To confirm full lock the RF Channel Status Register should be polled a number of times following the first interrupt to makes sure the detect flag is stable. This process is consistent with this type of integer-N synthesiser design where the first lock will overshoot but settles in time.

Alternatively, the two pairs of N and R registers can be used to rapidly switch from one set of N/R settings to another. This is useful when switching between transmit and receive as quickly as possible. The PE0201 kit was been used at 3V throughout.

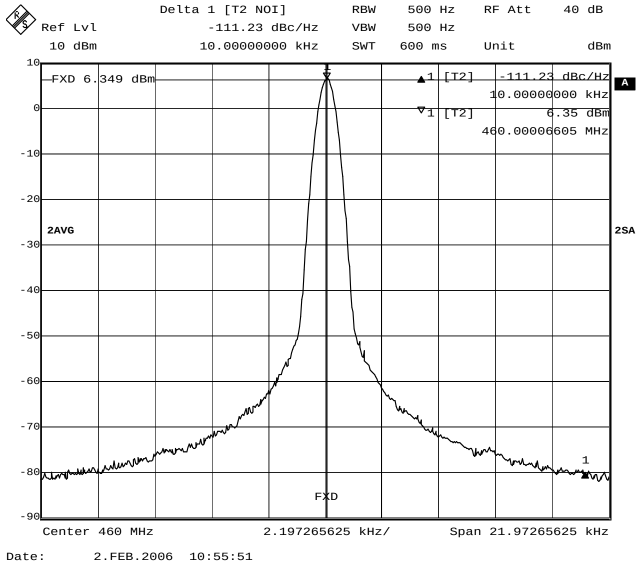

Figure 1 - Phase noise at 460MHz

Note: Minimum requirement was a 3V VCO design based on EN 300 113 limits for 12.5kHz channels; ACRR = 60dB, Bandwidth = 37dBHz, C/I = 12dB, giving -109dBc/Hz or better

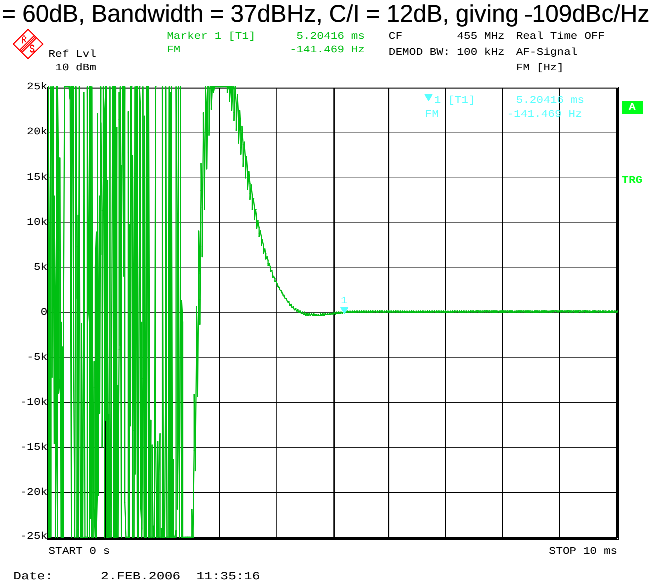

Figure 2 - Lock Time from 465MHz to 455MHz (Fcomp = 25kHz) = 5.2ms

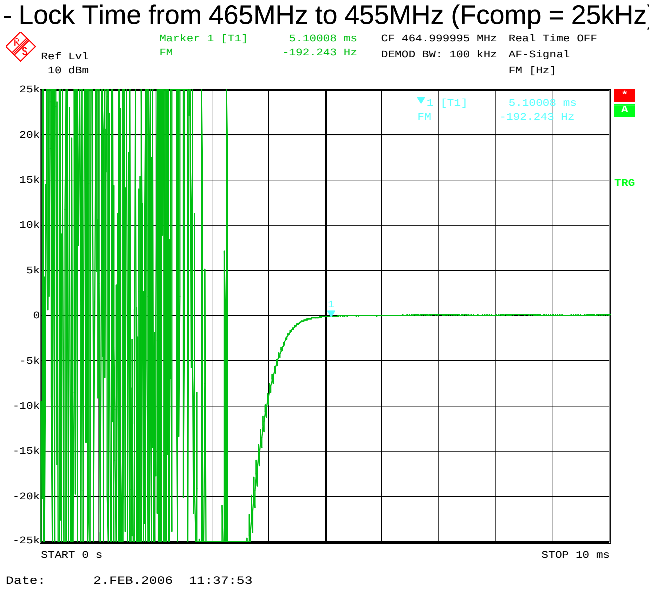

Figure 3 - Lock Time from 455MHz to 465MHz (Fcomp = 25kHz) = 5.1ms

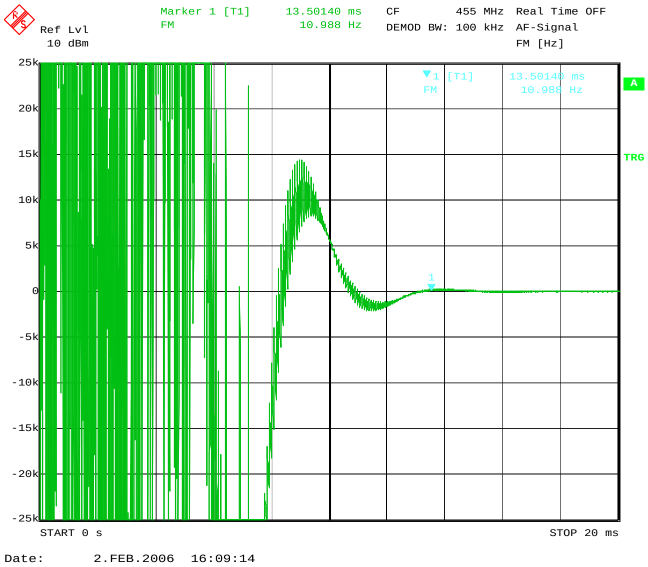

Figure 4 - Lock Time from 465MHz to 455MHz (Fcomp = 12.5kHz) = 13.5ms

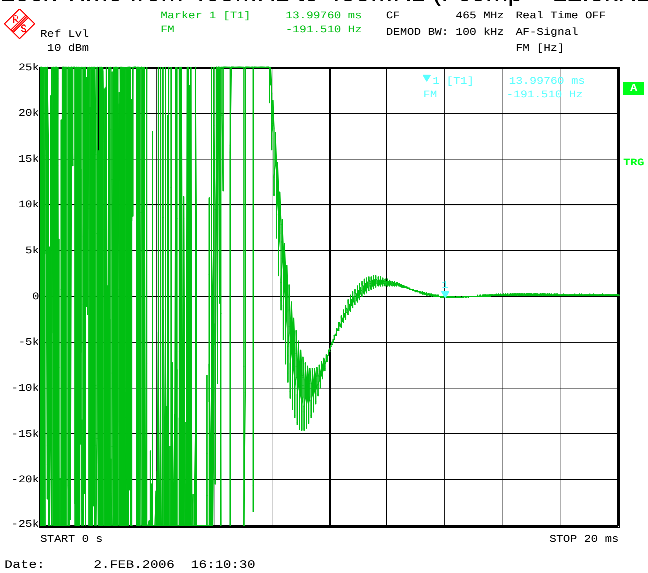

Figure 5 - Lock Time from 455MHz to 465MHz (Fcomp = 12.5kHz) = 14ms

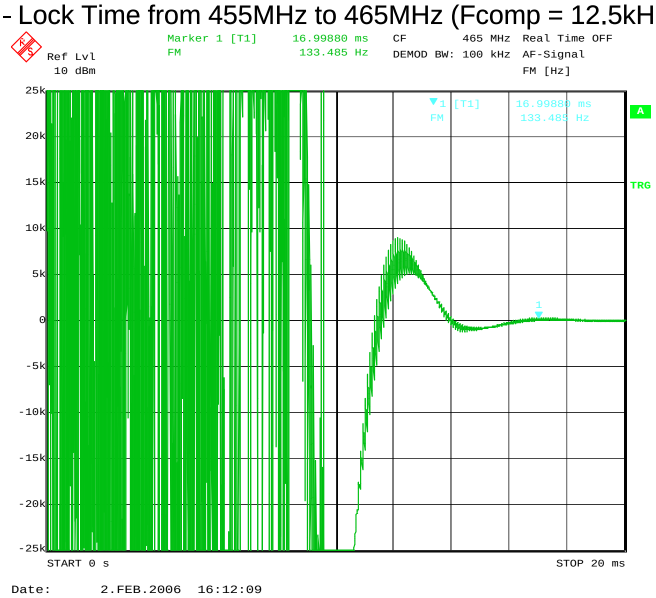

Figure 6 - Lock Time from unlocked (circa 435MHz) to 465MHz with Fcomp = 12.5kHz

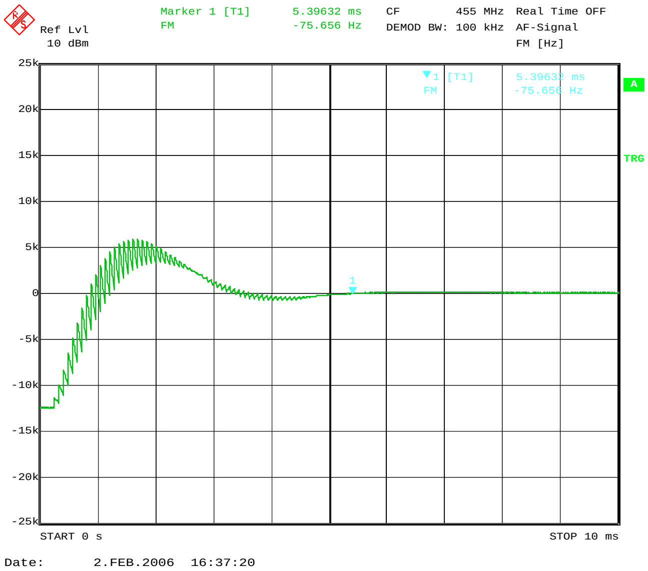

Figure 7 - Lock from 455MHz to 455.0125MHz (12.5kHz Fcomp) = 5.4ms

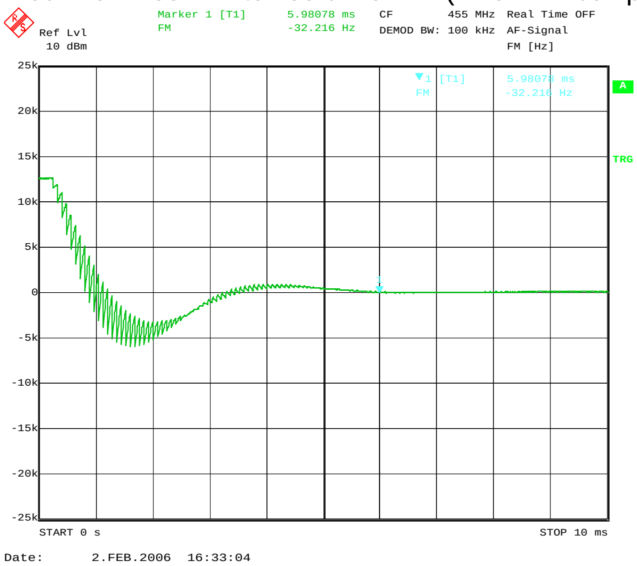

Figure 8 - Lock from 455.0125MHz to 455MHz (12.5kHz Fcomp) = 6ms

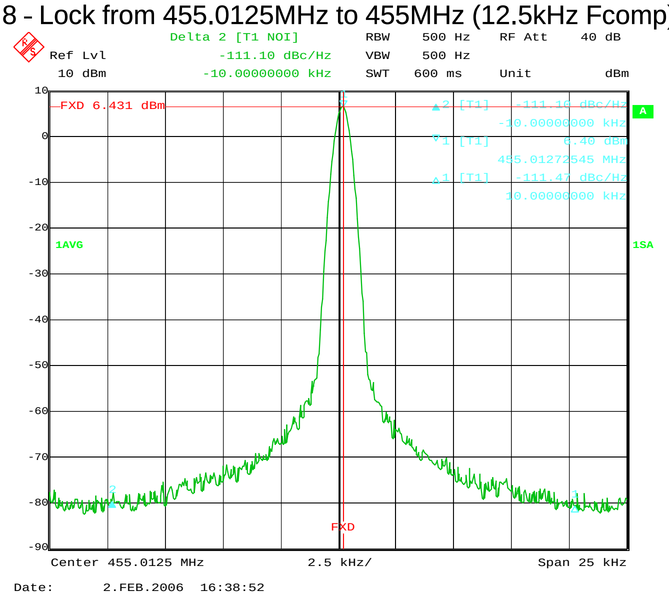

Figure 9 - Spectrum with 12.5kHz Reference at 455.0125MHz

3 Appendix

Scripts used for the above evaluation are as follows:

```
// route xtal input (19.2MHz) to RF synthesisers
W16 b3 8000

// Power nothing
W16 c0 0021

// Comparison frequency = 25kHz
// Tx Frequency = 455MHz
// Tx N divider = 18,200 = 0x4718
// Tx R divider =    768 = 0x0300
W16 b2 4318
W16 b2 4411
W16 b2 4B00
W16 b2 4C00

// Rx Frequency =  465MHz
// Rx N divider = 18,600 = 0x48A8
// Rx R divider =    768 = 0x0300
W16 b2 50A8
W16 b2 5412
W16 b2 5B00
W16 b2 5C00
// output Rx frequency
W16 b3 802d

// Rx Frequency =  460MHz
// W16 b2 53E0
// W16 b2 5411
// W16 b2 5B00
// W16 b2 5C00
// output Rx frequency
// W16 b3 802b

// Rx Frequency = 455MHz, Comparison Freq=12.5kHz
w16 b2 5A00
w16 b2 5C01
w16 b2 5230
w16 b2 5423
// output Tx frequency
// W16 b3 802b

// Tx Frequency = 465MHz, Comparison Freq=12.5kHz
// w16 b2 4A00
// w16 b2 4C01
// w16 b2 4150
// w16 b2 4424

// Tx Frequency = 455.0125MHz, Comparison Freq=12.5kHz
w16 b2 4A00
w16 b2 4C01
w16 b2 4231
w16 b2 4423
//output Tx frequency
W16 b3 802b
```

Note: Please refer to the PE0001 and PE0201 documentation for more details on how to use the scripts).

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For a full data sheet listing see: http://www.cmlmicro.com/products/datasheets/download.htm

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