

### Direct Conversion Receiver DATASHEET

D/994EF/1.0 April 2026

Provisional

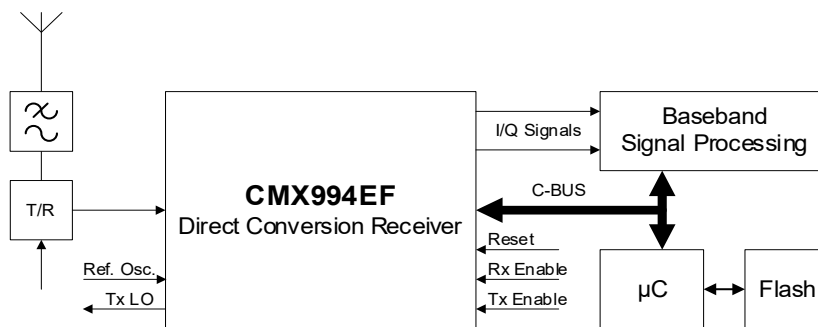
### Features

- **Replacement for Direct conversion receiver family**
  - CMX994 - Standard and low power mode
  - CMX994A - Standard and additional low power modes
  - CMX994E - Enhanced, standard and low power modes
  - CMX994G - Enhanced, 30 MHz guaranteed performance
- **Rx single conversion to zero IF, near-zero IF or low IF; zero IF eliminates image responses**
- **Very high mixer IIP2 for practical zero IF receiver**
- **100 MHz to 1 GHz I/Q demodulator**  
Extended operation down to 30 MHz
- **LNA with gain control**
- **Local Oscillator**
  - LO synthesiser
  - VCO negative resistance amplifier
  - Rx LO divide by 2, 4 or 6 modes
  - Tx LO Output with divide by 1, 2, 4, or 6 modes

- **Precise filtering with 1:2:4 bandwidth select control**
- **3.0 V – 3.6 V Low power Operation**
- **Small size 40-pin VQFN Package**

### Applications

- **Analogue/digital multi-mode radio**
- **Software Defined Radio (SDR)**
- **Data telemetry modems**
- **Satellite communications**
- **Constant envelope and linear modulation**
- **Rx function compatible with CMX998 Cartesian Feedback Loop Transmitter**
- **Narrowband e.g. 25 kHz, 12.5 kHz, 6.25 kHz**
- **Wideband Data e.g. >1 MHz bandwidth**



## 1 Brief Description

The CMX994EF replaces the prior generation of direct conversion receiver ICs from CML. CMX994EF has improved PowerTrade™, the ability to dynamically select power vs. performance modes to optimise operating trade-offs. The CMX994EF includes a broadband LNA with gain control followed by a high dynamic range, very high IIP2, I/Q demodulator. The receiver baseband section includes amplifiers and precise, configurable bandwidth, baseband filter stages. LO generation is provided by an integer-N PLL and a VCO negative resistance amplifier; an external LO may also be used. LO dividers are provided for flexible multi-band operation. The devices operate from a single 3.3 V supply over a temperature range of –40°C to +85°C and are available in a small 40-pin VQFN (Q4) package.

The CMX994EF includes all the advanced features of the CMX994A and CMX994E including the enhanced performance mode. The CMX994EF has a better transient response on power up/down allowing faster switching on/off allowing improved power-saving capability and operation in TDMA systems, improved LNA performance at frequencies >600 MHz and reduced power consumption specifically at higher operating frequencies.

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## 2 History

| Version | Changes                                                   | Date       |
|---------|-----------------------------------------------------------|------------|
| 1       | First published document at Provisional status for launch | April 2026 |

Information in this document is subject to change and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues.

It is recommended that you check for the latest product datasheet version from the Product page of the CML website: [<https://cmlmicro.com/>].

### 3 Block Diagram

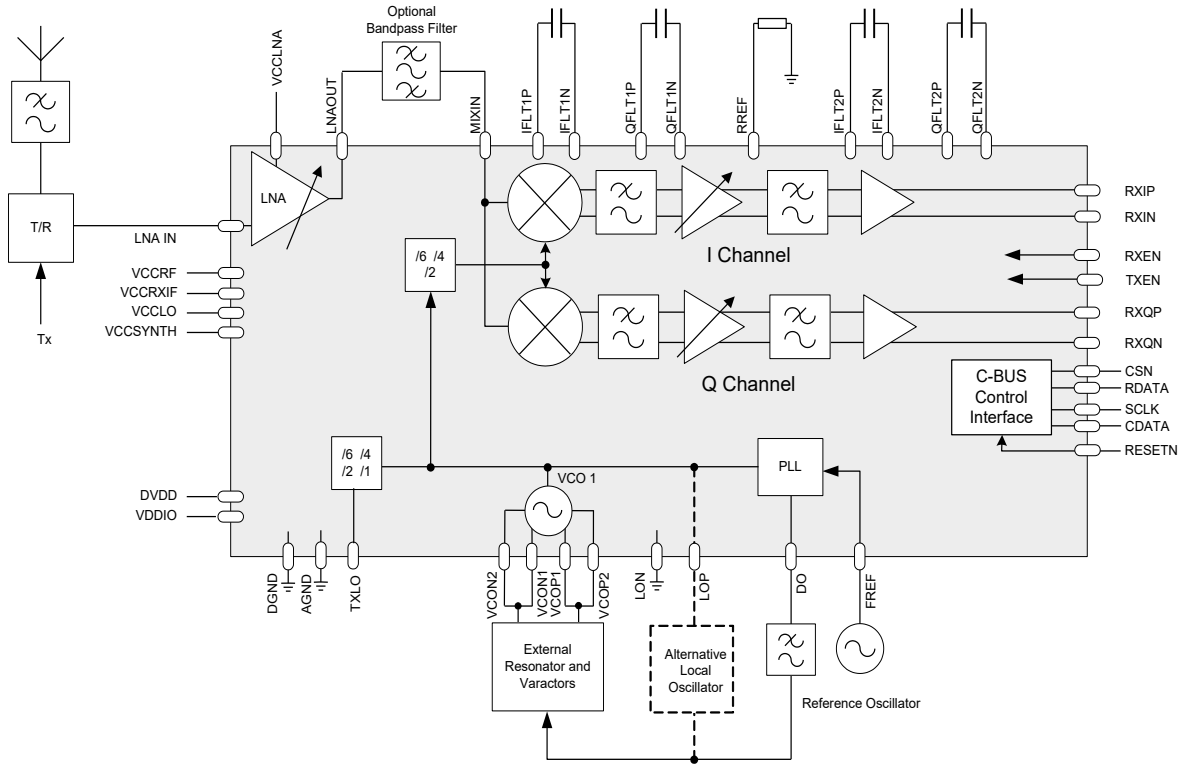


Figure 1 - Block Diagram

## 4 Pin and Signal List

| Pin No            | Pin Name | Type | Pin Function                                                             |
|-------------------|----------|------|--------------------------------------------------------------------------|
| 1                 | IFLT2N   | IP   | I channel 2 <sup>nd</sup> filter capacitor negative                      |
| 2                 | IFLT1P   | IP   | I channel 1 <sup>st</sup> filter capacitor positive                      |
| 3                 | IFLT1N   | IP   | I channel 1 <sup>st</sup> filter capacitor negative                      |
| 4                 | VCCRIF   | PWR  | Supply for baseband circuits                                             |
| 5                 | VCCLNA   | PWR  | Supply for LNA                                                           |
| 6                 | LNAIN    | IP   | LNA input                                                                |
| 7                 | LNAOUT   | OP   | LNA output                                                               |
| 8                 | VCCRF    | PWR  | Supply for RF circuits                                                   |
| 9                 | MIXIN    | IP   | Rx mixer input                                                           |
| 10                | TXLO     | OP   | LO output for Tx                                                         |
| 11                | VCCLO    | PWR  | Supply for LO sections                                                   |
| 12                | LOP      | IP   | PLL LO positive input                                                    |
| 13                | LON      | IP   | PLL LO negative input                                                    |
| 14                | VCOP1    | IP   | PLL VCO positive input 1                                                 |
| 15                | VCOP2    | IP   | PLL VCO positive input 2                                                 |
| 16                | VCON1    | IP   | PLL VCO1 negative input 1                                                |
| 17                | VCON2    | IP   | PLL VCO1 negative input 2                                                |
| 18                | VCCSYNTH | PWR  | Supply to Integer N PLL                                                  |
| 19                | FREF     | IP   | Reference frequency input                                                |
| 20                | DO       | OP   | PLL Charge Pump output                                                   |
| 21                | DGND     | PWR  | Digital ground                                                           |
| 22                | TXEN     | IP   | Tx Enable                                                                |
| 23                | RXEN     | IP   | Rx Enable                                                                |
| 24                | CSN      | IP   | C-BUS Chip Select                                                        |
| 25                | RDATA    | TSOP | C-BUS Data output                                                        |
| 26                | SCLK     | IP   | C-BUS Clock input                                                        |
| 27                | CDATA    | IP   | C-BUS Data input                                                         |
| 28                | RESETN   | IP   | C-BUS/Device Reset (Reset when pin Low)                                  |
| 29                | DVDD     | PWR  | Supply to digital circuits                                               |
| 30                | VDDIO    | PWR  | Supply to C-BUS circuits                                                 |
| 31                | RREF     | IP   | Reference resistor for I/Q Filters                                       |
| 32                | QFLT1N   | IP   | Q channel 1 <sup>st</sup> filter capacitor negative                      |
| 33                | QFLT1P   | IP   | Q channel 1 <sup>st</sup> filter capacitor positive                      |
| 34                | QFLT2N   | IP   | Q channel 2 <sup>nd</sup> filter capacitor negative                      |
| 35                | QFLT2P   | IP   | Q channel 2 <sup>nd</sup> filter capacitor positive                      |
| 36                | RXQP     | OP   | RxQ positive output                                                      |
| 37                | RXQN     | OP   | RxQ negative output                                                      |
| 38                | RXIP     | OP   | RxI positive output                                                      |
| 39                | RXIN     | OP   | RxI negative output                                                      |
| 40                | IFLT2P   | IP   | I channel 2 <sup>nd</sup> filter capacitor positive                      |
| EXPOSED METAL PAD | AGND     | PWR  | The exposed metal pad must be electrically connected to analogue ground. |

Total = 41 Pins (40 pins and central, exposed metal ground pad)

|               |     |   |               |     |   |                |
|---------------|-----|---|---------------|-----|---|----------------|
| <b>Notes:</b> | I/P | = | Input         | T/S | = | 3-state Output |
|               | O/P | = | Output        | NC  | = | No Connection  |
|               | BI  | = | Bidirectional | PWR | = | Power          |

## 4.1 Signal Definitions

**Table 1 - Definition of Power Supply and Reference Voltages**

| Signal Name     | Pins                                                  | Usage                                                     |
|-----------------|-------------------------------------------------------|-----------------------------------------------------------|
| $V_{max}$       |                                                       | The maximum value of the supplies $DV_{DD}$ and $AV_{DD}$ |
| $AV_{DD}$       | VCCRF, VCCRIF, VCCSYNTH,<br>VCCLO<br>VCLNA (see note) | Power supply for analogue circuits                        |
| $DV_{DD}$       | DVDD                                                  | Power supply for digital circuits                         |
| $VDD_{IO}$      | VDDIO                                                 | Power supply voltage for digital interface (C-BUS)        |
| $DV_{SS}$ (GND) | DGND                                                  | Ground for digital circuits                               |
| $AV_{SS}$ (GND) | AGND                                                  | Ground for analogue circuits                              |

Note: The LNA has a separate power connection pin to provide isolation of non-differential signals. This may be connected to a common external supply with suitable de-coupling.

## 4.2 Connection of Unused Pins

If the CMX994EF VCO and PLL functions are not used then pins FREF, DO, VCOP1, VCOP2, VCON1 and VCON2 may be left unconnected.

## 5 External Components

### 5.1 Power Supply and Decoupling

The CMX994EF have separate supply pins for the analogue and digital circuitry; a 3.3 V nominal supply is recommended for all circuits but the data interface can run at a lower voltage than the rest of the device by setting the VDD<sub>IO</sub> supply to the required interface voltage.

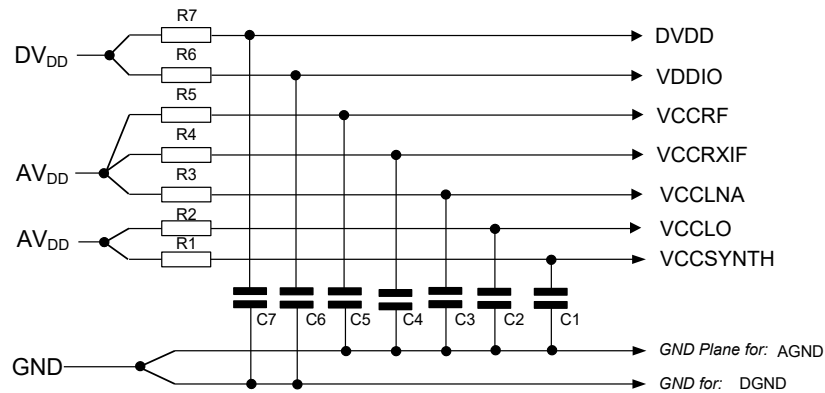


Figure 2 - Recommended Power Supply Connections and Decoupling

Table 2 - Decoupling Components

|    |              |  |    |              |
|----|--------------|--|----|--------------|
| C1 | 10 nF        |  | R1 | 10 $\Omega$  |
| C2 | 10 nF        |  | R2 | 3.3 $\Omega$ |
| C3 | 33 pF//10 nF |  | R3 | 3.3 $\Omega$ |
| C4 | 10 nF        |  | R4 | 3.3 $\Omega$ |
| C5 | 10 nF        |  | R5 | 3.3 $\Omega$ |
| C6 | 10 nF        |  | R6 | 10 $\Omega$  |
| C7 | 10 nF        |  | R7 | 10 $\Omega$  |

#### Notes:

1. Maximum Tolerances: Resistors  $\pm 5\%$ , capacitors  $\pm 20\%$ .
2. It is expected that any low-frequency interference on the 3.3 Volt supply will be removed by active regulation; a large capacitor is an alternative but may require more board space and so may not be preferred. It is particularly important to ensure that there is no interference from the VDD<sub>IO</sub> (which supplies the digital I/O) or from any other circuit that may use the DVDD supply (such as a microprocessor), to sensitive analogue supplies (AVDD). It is therefore advisable to use separate power supplies for digital and analogue circuits.
3. The supply decoupling shown is intended for RF noise suppression. It is necessary to have a small series impedance prior to the decoupling capacitor for the decoupling to work well. This may be achieved cost effectively by using the resistor and capacitor values shown. The use of resistors results in small dc voltage drops (up to approx. 0.1 V). Choosing resistor values approximately inversely proportional to the dc current requirements of each supply ensures the dc voltage drop on each supply is reasonably matched. In any case, the resultant dc voltage change is well within the design tolerance of the device. If higher impedance resistors are used (not recommended) then greater care will be needed to ensure the supply voltages are maintained within tolerance, even when parts of the device are enabled or disabled.
4. It is advisable to have separate ground planes for analogue and digital circuits.
5. Separate regulators for local oscillator sections (VCCLO, VCCSYNTH) may be beneficial depending on circuit noise and type of regulator and this is why two AVDD connections are shown.

## 5.2 Receiver

### 5.2.1 LNA

The following sections show plots and tables of the LNA input ( $S_{11}$ ) and output ( $S_{22}$ ) impedance. Separate data is shown for the 50  $\Omega$  and 100  $\Omega$  output modes which are selected by LNAZ<sub>0</sub> bit in the Rx Gain Register (b3, \$16; see section 7.7.1).

Note that at low frequencies capacitive loads on the LNA output are not recommended, a high-pass matching network is preferred. A s2p file of the LNA unmatched in both 50  $\Omega$  and 100  $\Omega$  mode can be downloaded from the CML Micro website for development of matching networks.

#### 50 $\Omega$ Mode

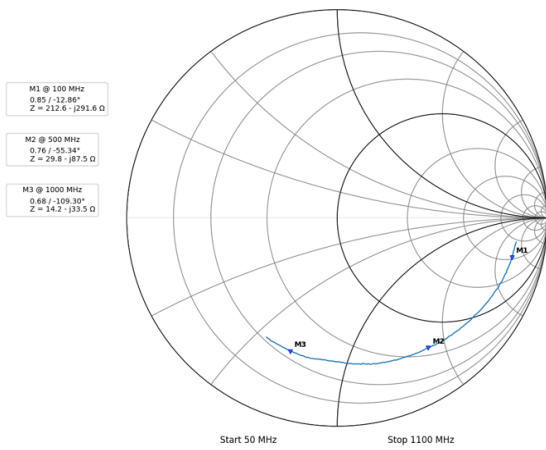


Figure 3 - LNA  $S_{11}$  (50  $\Omega$  Mode)

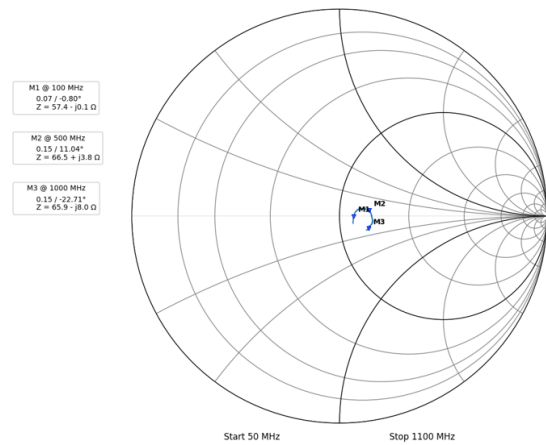
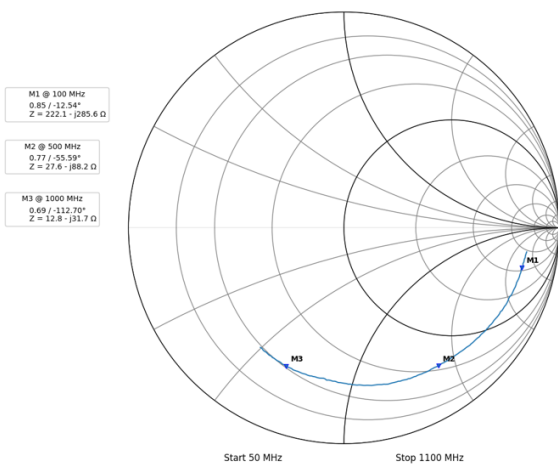


Figure 4 - LNA  $S_{22}$  (50  $\Omega$  Mode)

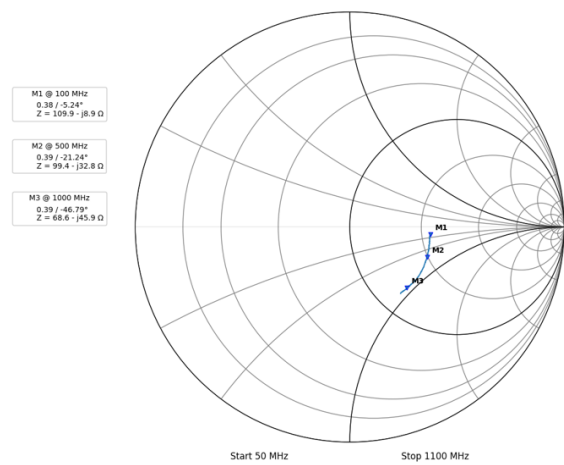
**Table 3 - LNA S<sub>11</sub> and S<sub>22</sub> Impedances and Parallel Equivalent Circuit in 50 Ω Mode**

| Freq (MHz) | S <sub>11</sub>    |                                    | S <sub>22</sub>    |                                    |
|------------|--------------------|------------------------------------|--------------------|------------------------------------|
|            | Impedance (Ω-/+jΩ) | Equivalent Parallel Circuit (R//C) | Impedance (Ω-/+jΩ) | Equivalent Parallel Circuit (R//C) |
| 50         | 367.8 – j322.9     | 651R // 4.2 pF                     | 56.9 – j4          | 57R // 4 pF                        |
| 100        | 212.6 – j291       | 613R // 3.5 pF                     | 57.4 – j0.1        | 57R                                |
| 150        | 134.6 – j245.9     | 584R // 3.4 pF                     | 58 + j1.7          | 58R                                |
| 200        | 90.6 – j199.5      | 530R // 3.3 pF                     | 59 + j3            | 59R                                |
| 250        | 67.2 – j165.5      | 475R // 3.3 pF                     | 60.2 + j4.2        | 60R                                |
| 300        | 54.7 – j143.5      | 431R // 3.3 pF                     | 60.9 + j4.3        | 61R                                |
| 350        | 44.9 – j123.9      | 387R // 3.3 pF                     | 62.3 + j4.4        | 62R                                |
| 400        | 37.5 -j108.1       | 349R // 3.3 pF                     | 63.8 + j4.7        | 64R                                |
| 450        | 32.5 – j96.5       | 319R // 3.3 pF                     | 65.3 + j4.4        | 66R                                |
| 500        | 29.8 – j87.5       | 283R // 3.3 pF                     | 66.5 + j3.8        | 67R                                |
| 550        | 26.6 – j79.3       | 263R // 3.3 pF                     | 67.2 + j2.7        | 67R                                |
| 600        | 24.2 – j71.9       | 238R // 3.3 pF                     | 68 + j1.4          | 68R                                |
| 650        | 22.2 – j65.9       | 217R // 3.3 pF                     | 68.5 – j0.3        | 68R                                |
| 700        | 20.5 – j59.6       | 194R // 3.4 pF                     | 68.8 – j2          | 69R                                |
| 750        | 19.3 – j54.2       | 171R // 3.5 pF                     | 68.9 – j3.4        | 69R                                |
| 800        | 18.3 – j49.8       | 154R //3.5 pF                      | 68.7 – j4.2        | 69R                                |
| 850        | 17.4 – j45.4       | 136R // 3.6 pF                     | 68 – j5.6          | 68R                                |
| 900        | 16.2 – j41.2       | 121R // 3.7 pF                     | 66.6 – j6.8        | 67R                                |
| 950        | 15 – j37.4         | 108R // 3.9 pF                     | 65.9 – j7.1        | 67R                                |
| 1000       | 14.2 – j33.5       | 92R // 4 pF                        | 65.9 – j8          | 67R                                |

**100Ω Mode**



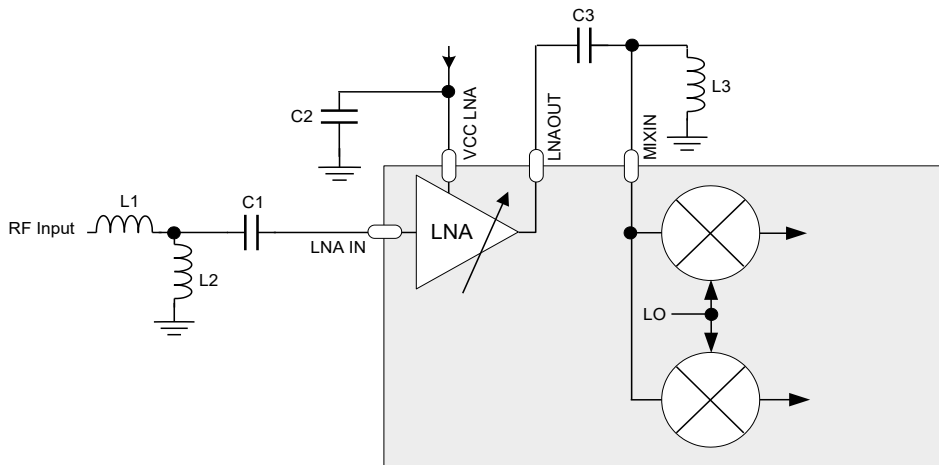
**Figure 5 - LNA S<sub>11</sub> (100 Ω Mode)**



**Figure 6 - LNA S<sub>22</sub> (100 Ω mode)**

**Table 4 - LNA S<sub>11</sub> and S<sub>22</sub> Impedances and Parallel Equivalent Circuit in 100 Ω Mode**

| Freq (MHz) | S <sub>11</sub>    |                                    | S <sub>22</sub>    |                                    |
|------------|--------------------|------------------------------------|--------------------|------------------------------------|
|            | Impedance (Ω-/+jΩ) | Equivalent Parallel Circuit (R//C) | Impedance (Ω-/+jΩ) | Equivalent Parallel Circuit (R//C) |
| 50         | 367.9 – j313.4     | 638R // 4.1 pF                     | 109.9 – j7.6       | 110R // 2 pF                       |
| 100        | 222.1 – j286       | 589R // 3.4 pF                     | 109.9 – j8.9       | 111R // 1.1 pF                     |
| 150        | 141.3 – j244       | 563R // 3.3 pF                     | 108.5 – j10.9      | 110R // 1 pF                       |
| 200        | 94 – j200.8        | 523R // 3.3 pF                     | 108 – j14.4        | 110R // 0.9 pF                     |
| 250        | 67.7 – j168.6      | 487R // 3.2 pF                     | 106.7 – j17.8      | 110R // 0.9 pF                     |
| 300        | 52.4 – j143.4      | 444R // 3.2 pF                     | 105.6 – j21        | 110R // 0.9 pF                     |
| 350        | 43.8 – j126        | 406R // 3.2 pF                     | 104.9 – j24.3      | 110R // 0.9 pF                     |
| 400        | 36.5 – j110.2      | 369R // 3.2 pF                     | 103.2 – j27.2      | 110R // 0.9 pF                     |
| 450        | 31.9 – j98.8       | 338R // 3.3 pF                     | 101 – j29.9        | 110R // 0.9 pF                     |
| 500        | 27.6 – j88.2       | 307R // 3.3 pF                     | 99.4 – j32.8       | 110R // 0.9 pF                     |
| 550        | 24.2 – j79.2       | 282R // 3.3 pF                     | 96.2 – j35.8       | 110R // 0.9 pF                     |
| 600        | 21.6 – j71.3       | 258R // 3.3 pF                     | 92.9 – j38.5       | 109R // 1 pF                       |
| 650        | 19.6 – j64.9       | 235R // 3.4 pF                     | 90.6 – j40.3       | 109R // 1 pF                       |
| 700        | 18.1 – j58.6       | 208R // 3.5 pF                     | 87.3 – j42.6       | 108R // 1 pF                       |
| 750        | 16.8 – j52.8       | 183R // 3.6 pF                     | 83.8 – j43.9       | 107R // 1 pF                       |
| 800        | 16 – j48.1         | 161R // 3.7 pF                     | 80.7 – j44.7       | 106R // 1 pF                       |
| 850        | 15.2 – j43.3       | 138R // 3.8 pF                     | 77.7 – j45.7       | 105R // 1 pF                       |
| 900        | 14.3 – j39.1       | 121R // 3.9 pF                     | 74 – j45.9         | 103R // 1 pF                       |
| 950        | 13.5 – j35.6       | 107R // 4.1 pF                     | 71.6 – j45.8       | 101R // 1 pF                       |
| 1000       | 12.8 – j31.7       | 89R // 4.3 pF                      | 68.6 – j45.9       | 99R // 1 pF                        |



**Figure 7 - Recommended LNA Configuration and Inter-stage Match**

**Table 5 - 150 MHz LNA and Inter-stage Components (100 Ω output mode)**

|    |                |    |                    |
|----|----------------|----|--------------------|
| C1 | 1 nF           | L1 | 150 nH             |
| C2 | 33 pF // 10 nF | L2 | 2.7 pF (capacitor) |
| C3 | 18 pF          | L3 | 150 nH             |

**Table 6 - 450 MHz LNA and Inter-stage Components**

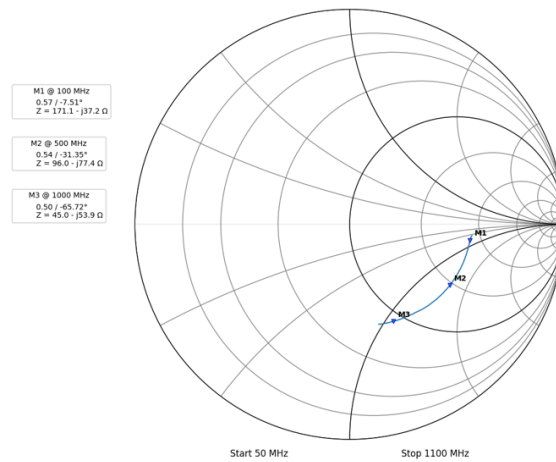
|    |                |    |       |
|----|----------------|----|-------|
| C1 | 1 nF           | L1 | 39 nH |
| C2 | 33 pF // 10 nF | L2 | 82 nH |
| C3 | 10 pF          | L3 | 27 nH |

**Table 7 - 1000 MHz LNA and Inter-stage Components (50  $\Omega$  output mode)**

|    |               |    |        |
|----|---------------|----|--------|
| C1 | 100 pF        | L1 | 12 nH  |
| C2 | 33 pF //10 nF | L2 | 8.7 nH |
| C3 | 4.7 pF        | L3 | 5.6 nH |

### 5.2.2 Mixers and Baseband Section

Figure 8 is a plot of the typical Rx Mixer input impedance; Table 8 gives the measured impedances and the equivalent parallel circuit at some particular frequencies. A s1p file of the mixer input unmatched can be downloaded from the CML Micro website for development of matching networks.

**Figure 8 - Rx Mixer Input Impedance****Table 8 - CMX994EF Rx Mixer Input Impedances and Parallel Equivalent Circuit**

| Frequency (MHz) | Impedance ( $\Omega$ -/+j $\Omega$ ) | Parallel Equivalent Circuit (R // pF) |
|-----------------|--------------------------------------|---------------------------------------|
| 50              | 178.8 - j27.9                        | 183R // 2.7 pF                        |
| 100             | 171.2 - j37.2                        | 179R // 1.9 pF                        |
| 150             | 164.2 - j46.9                        | 178R // 1.7 pF                        |
| 200             | 155 - j56.9                          | 176R // 1.7 pF                        |
| 250             | 144.6 - j65                          | 174R // 1.6 pF                        |
| 300             | 135.4 - j70.3                        | 172R // 1.6 pF                        |
| 350             | 124.4 - j75                          | 169R // 1.6 pF                        |
| 400             | 114 - j76.8                          | 166R // 1.6 pF                        |
| 450             | 104 - j77.5                          | 162R // 1.6 pF                        |
| 500             | 96 - j77.4                           | 158R // 1.6 pF                        |
| 550             | 87.8 - j76.4                         | 154R // 1.6 pF                        |
| 600             | 80.3 - j74.8                         | 150R // 1.6 pF                        |
| 650             | 74.5 - j72.9                         | 146R // 1.6 pF                        |
| 700             | 68.6 - j70.3                         | 141R // 1.7 pF                        |
| 750             | 63.2 - j67.5                         | 135R // 1.7 pF                        |
| 800             | 59.1 - j64.8                         | 130R // 1.7 pF                        |
| 850             | 55 - j62                             | 125R // 1.7 pF                        |
| 900             | 51.3 - j59.1                         | 119R // 1.7 pF                        |
| 950             | 48.2 - j56.7                         | 115R // 1.7 pF                        |
| 1000            | 45 - j53.9                           | 109R // 1.7 pF                        |

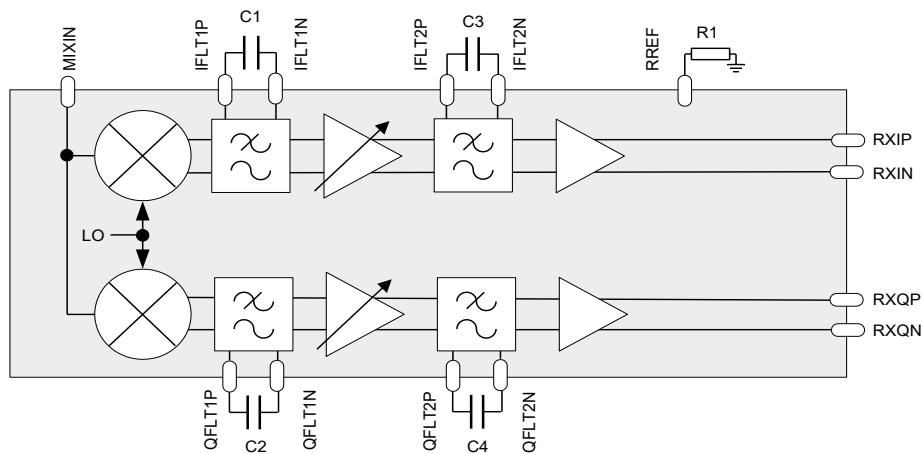


Figure 9 - Recommended Receiver Filter Circuit values

Table 9 - Receiver Filter Components

|    |        |    |               |
|----|--------|----|---------------|
| C1 | 1.5 nF | C4 | 3.9 nF        |
| C2 | 1.5 nF | R1 | 10 k $\Omega$ |
| C3 | 3.9 nF |    |               |

The bandwidth of the first baseband filters is set by capacitors C1 and C2. Capacitors C3 and C4 together with the reference resistor R1 set the bandwidth of the second baseband filters. Component selection will vary depending on the desired filter bandwidths. For further details see sections 6.2.2 and 6.2.3.

## 5.3 Local Oscillator

### 5.3.1 Local Oscillator Input

LON and LOP signals form a differential signal pair however the LO input may be driven by a single-ended source, in which case pin LOP should be connected to the LO signal and LON may be connected directly to ground. The inputs have internal ac coupling, so external dc blocking capacitors are not required.

### 5.3.2 VCO and PLL

A typical configuration for using the internal VCO negative resistance amplifier at 440 MHz is shown in Figure 10. For the other external components required to complete the PLL (the loop filter components) see Figure 11 which shows a third-order loop filter. Typical values for a 500 Hz bandwidth are given in Table 11.

VCOP1 should be shorted directly to VCOP2 and similarly VCON1 to VCON2 in order to form the negative resistance loop. It is recommended that the parallel LC tank (L1/C1) is situated as close to the package as possible, with the L closest to the device pins. Also, the shorting of VCOP1 to VCOP2 and of VCON1 to VCON2 occurs as close as possible to the tank circuit – this minimises the effects of series inductance on the oscillator behaviour.

The reference frequency input, FREF, should use an external dc blocking capacitor.

**Note:** The CMX994EF is more sensitive to the Q of the inductor (L1) than previous members of the CMX994x family, a Q > 50 is recommended

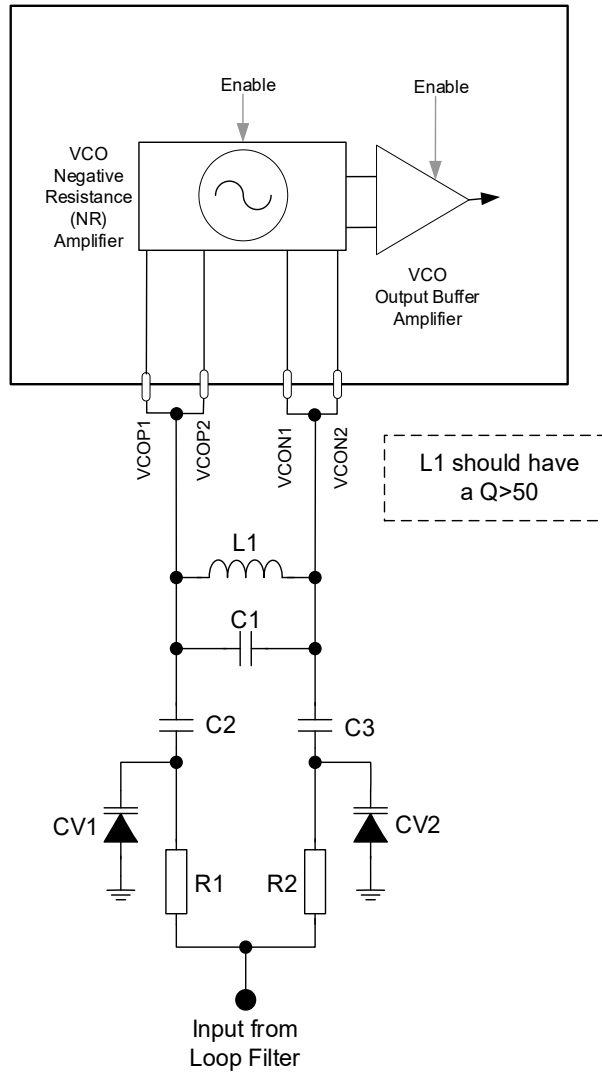


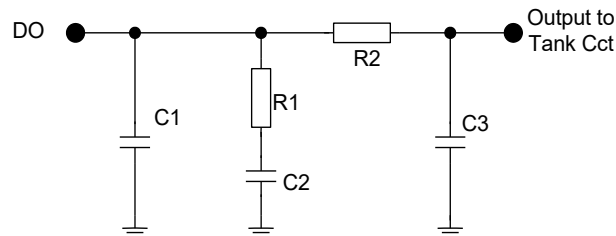
Figure 10 - Example External Components – VCO External Tank Circuit

**Table 10 - Internal VCO Amplifier Tank Circuit for 440 MHz Operation**

|    |                 |     |               |
|----|-----------------|-----|---------------|
| L1 | 8.2 nH (Note 1) | CV1 | SMV1705-079LF |
| C1 | 8.2 pF (Note 2) | CV2 | SMV1705-079LF |
| C2 | 22 pF           | R1  | 10 k $\Omega$ |
| C3 | 22 pF           | R2  | 10 k $\Omega$ |

Note 1: Tolerance of 2% or better recommended

Note 2: Tolerance of 5% or better recommended

**Figure 11 - Example External Components – PLL Loop Filter****Table 11 - 3rd Order Loop Filter Circuit Values**

|    |         |    |                |
|----|---------|----|----------------|
| C1 | 150 nF  | R1 | 1.5 k $\Omega$ |
| C2 | 1000 nF | R2 | 2.4 k $\Omega$ |
| C3 | 15 nF   |    |                |

## 5.4 RESETN

The RESETN pin generates a reset signal when low. The RESETN pin has an internal pull-up resistor of 100 k $\Omega$  connected to VDD<sub>IO</sub>.

## 6 General Description

The architecture of the CMX994EF devices is shown in Figure 1. The CMX994EF is a receiver IC featuring very high IIP2 I/Q demodulators intended for use as a direct conversion receiver to zero IF, near-zero IF and low IF. The device has flexible LO inputs, integer-N PLL and an on-chip negative resistance amplifier which, with the addition of suitable external components, provides a VCO.

The receiver is fully integrated with a Low Noise Amplifier (LNA) preceding the down-converter section. The LNA may be configured with one of two possible output impedance settings (100  $\Omega$  or 50  $\Omega$ ). With the 50  $\Omega$  mode selected, there is more gain available, but the circuit will consume an additional 2 mA of current. The 50  $\Omega$  mode has primarily been included for use at frequencies of 450 MHz or higher. It should be noted that as the output impedance is not the same for each setting, the required matching components between the LNA and mixer will potentially need to be different for each case for optimal performance.

The high-linearity down-converting mixers are immediately followed by a baseband filter stage. The bandwidth of this section is set by external capacitors. This first stage of filtering is designed to remove off-channel blocking signals prior to baseband amplification. Following these filters, gain is applied via a variable gain amplifier. Further filtering is then applied and again the bandwidth of the filters is determined by external capacitors. A reference resistor must also be fitted; this is used to calibrate the internal filter circuits to ensure the cut-off point of the filters is accurately controlled. This system allows effective correction for the analogue response to be applied in signal processing following the CMX994EF. The output of the CMX994EF is differential I/Q signals; these may be applied to analogue-to-digital converters such as those in the CMX983, CMX7032, CMX7341, SCT3288, CMX7163 or the CMX7164 ICs.

The receiver I/Q chain includes the facility to correct for inherent dc offsets in the hardware. This process is intended to optimise the dynamic range of the system and must be controlled by the microprocessor or DSP that processes the I/Q signals from the CMX994EF. DC offsets are a well-known issue with direct conversion receivers. In dynamic signal environments dc offset removal algorithms will be required to track and remove dc offsets generated by off-channel signals. Very high I/Q mixer IIP2 performance minimises such offsets. The receiver sections have a low power mode that reduces current. This mode may be used when reduced intermodulation performance is acceptable.

The Local Oscillator section features an integer-N Phase Locked Loop (PLL). This may be used with the on-chip VCO or with an external VCO. The on-chip VCO consists of a negative resistance amplifier and buffers, which allows an external inductor together with external varactor diodes to determine the operating frequency and tuning range. The use of external components allows optimum phase noise to be achieved. The Rx LO signal may be divided by 2, 4 or 6. There is also a Tx LO output provided, and the Tx LO signal may be divided by 1, 2, 4 or 6. Alternatively the on-chip PLL and VCO can be disabled and an external LO source supplied.

All features of the CMX994EF may be controlled by the C-BUS control interface.

The following sections describe specific features of the CMX994EF.

## 6.1 General Operation

### 6.1.1 Rx/Tx Enable

The CMX994EF has Tx Enable and Rx Enable pins and the same function can be accessed via C-BUS using the General Control Register (section 7.2). The logical signals 'Tx ON' and 'Rx ON' are the ORed combination of the C-BUS signal and the hardware signals as shown in Table 12. Thus, either C-BUS or hardware enable signals may be used, with the unused mode being set to '0'.

**Table 12 - Tx (or Rx) Enable Operation**

| Tx (or Rx) Enable Pin | C-BUS Tx (or Rx) Enable | 'Tx ON' (or 'Rx ON') Result |
|-----------------------|-------------------------|-----------------------------|
| 0                     | 0                       | 0                           |
| 1                     | 0                       | 1                           |
| 0                     | 1                       | 1                           |
| 1                     | 1                       | 1                           |

'Tx ON' enables the following sections of the device:

- Tx divider (see also Figure 1 and section 7.11.1).

'Rx ON' enables the following sections of the device:

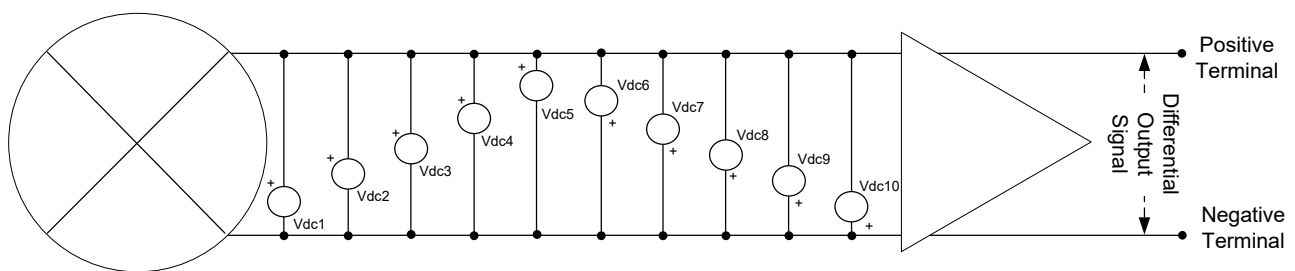
- LNA
- Down-converters and I/Q baseband amplifiers
- Rx LO divider

## 6.2 Receiver Operation

### 6.2.1 DC Offset Correction

Digitally controlled dc offset correction is provided which is capable of reducing the offset to 20 mV or less for errors of up to +/-640 mV. This represents a reduction in dynamic range of less than 0.1 dB for a typical ADC input signal range (2 V<sub>p-p</sub>) and is therefore negligible. The required correction must be measured externally as such measurements are application specific. The correction is applied close to the start of the I/Q baseband chain and therefore maximises dynamic range in the analogue sections.

The correction is applied in a differential manner so positive and negative corrections are possible; see Figure 12. This allows the dc to be corrected to the nominal dc bias level. The voltage sources are scaled in a binary fashion so multiple sources can be added to provide the desired correction. The same arrangement applies independently on both I and Q channels. In the CMX994EF the extra sources have been retained but the step size reduced from 25 mV to 20 mV to give an improved resolution.



**Figure 12 - Simplified Schematic of How DC Offset Corrections are Applied**

Table 13 - DC Offset Correction Adjustments

| Source | Voltage Correction at Output for Maximum Gain in Baseband Amplifiers | Correction Polarity                                    |
|--------|----------------------------------------------------------------------|--------------------------------------------------------|
| Vdc1   | 20 mV                                                                | Positive terminal increase, Negative terminal decrease |
| Vdc2   | 40 mV                                                                | Positive terminal increase, Negative terminal decrease |
| Vdc3   | 80 mV                                                                | Positive terminal increase, Negative terminal decrease |
| Vdc4   | 160 mV                                                               | Positive terminal increase, Negative terminal decrease |
| Vdc5   | 320 mV                                                               | Positive terminal increase, Negative terminal decrease |
| Vdc6   | 20 mV                                                                | Negative terminal increase, Positive terminal decrease |
| Vdc7   | 40 mV                                                                | Negative terminal increase, Positive terminal decrease |
| Vdc8   | 80 mV                                                                | Negative terminal increase, Positive terminal decrease |
| Vdc9   | 160 mV                                                               | Negative terminal increase, Positive terminal decrease |
| Vdc10  | 320 mV                                                               | Negative terminal increase, Positive terminal decrease |

### 6.2.2 Receiver Filters and Bandwidth Options

The I and Q channels incorporate two stages of filtering to reduce blocking signals and to attenuate nearby channels. This allows the wanted signal to be maximised without significant distortion being introduced as a result of unwanted larger signals saturating the later amplification stages.

The CMX994EF supports multiple channel bandwidths, providing scalable filtering in the baseband (I/Q) chain. Two filter stages are provided. The post mixer filter provides rejection of large off-channel signals such as those typically used in blocking tests. With this protection in place some gain is provided before narrower filters that provide rejection of the adjacent channel. Following this filter, the remainder of the receiver gain is provided. Both filter stages have single-pole characteristics, having -3 dB frequency points set by separate external capacitors.

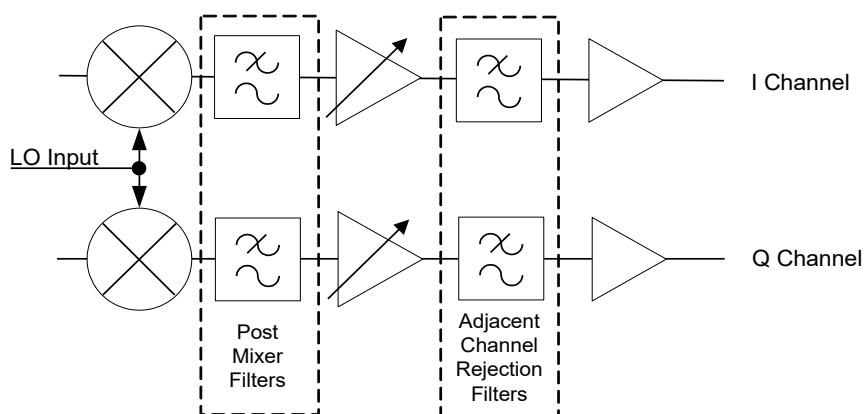


Figure 13 - Baseband I/Q Filtering

After setting the second filter stage bandwidth via external capacitors, the bandwidth can then be scaled under serial control to allow multiple channel bandwidths to be supported by the CMX994EF. A typical

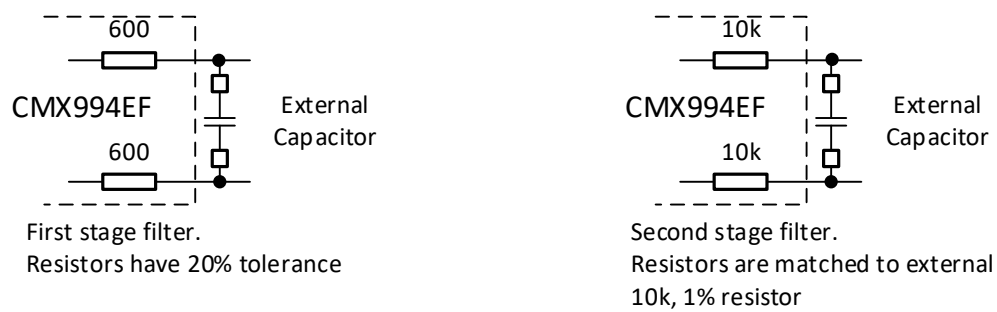
requirement is to support 6.25 kHz, 12.5 kHz and 25 kHz channels, so the scaling of the Adjacent Channel Rejection (ACR) filter is 1 : 2 : 4 via a bandwidth mode control. Using the recommended external capacitors for a 6.25 kHz design (see Table 11), the ACR filter bandwidth (-3 dB) is 2 kHz. This provides 9 dB rejection of the adjacent channel and 15dB rejection at 12.5 kHz. Using the bandwidth scaling control, the 2 kHz filter bandwidth can then be changed to 4 kHz or 8 kHz (see Rx Control Register, section 7.3), without changing external components. See also section 8.1.6.

The ACR filter may introduce some deterministic distortion in the signal passband, this distortion can be compensated by using filters external to the CMX994EF; see section 6.2.3 for further information.

The scaling of the post-mixer filter is less critical. The bandwidth (-3 dB), using the recommended values, is approximately 88 kHz (at maximum gain). This should be suitable for all the channel bandwidths up to 25 kHz, so no scaling is provided. Note that the bandwidth of this section will reduce by 30% (typ.) as gain is reduced in the baseband section.

### 6.2.3 Baseband Filter Design and Required Correction

The pole frequencies of the filter stages are set by the addition of external capacitors (see also Table 11); the resistors are internal to the chip and those on the second filter stage are trimmed so as to match the external 10 kΩ reference resistor<sup>1</sup>.



**Figure 14 - Schematic Representation of Filters used in the I and Q Paths**

Filtering close to the passband distorts the signal and increases the BER, so it is necessary to provide correction for the filter distortion in subsequent external digital filtering.

Both filter stages are single-pole filters. The first filter stage is designed to reduce blocking signals, and it will typically be set at 4 x the maximum required channel spacing. As a result, tolerance is not particularly critical, and it is usually not necessary to compensate the wanted signal for this filter. The second filter is designed to operate close to, or within, the passband. It is therefore important that compensation is provided for the wanted signal.

Different modulation schemes occupy different bandwidths within a channel, so optimisation of the filter positioning will vary depending on the modulation scheme. Some experimentation may be required to get the best results but, as a guide, the second filter stage should have its frequency set to between 30% and 40% of the channel spacing. The aim is to reduce adjacent and close-in channels as much as possible. Provided the filter effects are compensated for later, the lowering of the signal amplitude at the band edges is usually well tolerated, although the extent of this will depend on the modulation scheme used.

The CMX994EF allows up to three different channel spacings to be selected via the C-BUS interface. If, for example, the three channel spacings required are 6.25 kHz, 12.5 kHz and 25 kHz, then the first filter should be set at a nominal desired frequency to ensure large blocking signals are rejected, typically a cut off frequency around 100 kHz would be suitable. If only two channel spacings are required, of 6.25 kHz and 12.5 kHz for example, then it would be slightly beneficial to set the post mixer filter bandwidth to 50 kHz.

Note that the three channel spacings are always in a 1:2:4 ratio relative to the smallest channel spacing, which is set by external components.

<sup>1</sup> The external resistor should be 1% tolerance or better.

The second stage filter capacitor should be selected for the smallest bandwidth requirement. The calculation for the capacitor value is as follows:

$$C = \frac{1}{2\pi f 20,000}$$

Where  $f$  = filter pole frequency (-3 dB point).

Therefore, a capacitor of 4 nF would yield a frequency pole of 1989 Hz. This may be a typical figure when using a channel spacing of 6.25 kHz. To maintain the accuracy of the compensation the capacitor must have a low temperature coefficient and tolerance better than or equal to 2%.

A compensation filter would need to be applied in the digital domain having the inverse characteristic. This would be:

$$H(s) = 1 + \frac{s}{2\pi f}$$

This would normally be implemented as a FIR filter. It should be followed with another non-critical FIR that rolls off the signal when out of band. This second filter may be part of a required channel filter.

Selecting 2x or 4x bandwidth will require the compensation filter to be adjusted in proportion.

The first stage filter capacitor may be calculated in a similar way:

$$C = \frac{1}{2\pi f 1200}$$

Where  $f$  = filter pole frequency (-3 dB point).

Therefore, a capacitor of 1.5 nF would yield a frequency pole of approx. 88 kHz. This may be a typical figure if the maximum channel spacing required were 25 kHz. There is a wider tolerance on this, as the internal resistors are not trimmed. Consequently, it is not required to have a low tolerance value on the first stage filter capacitor.

Should it be required to have this closer to the passband then a correction filter may be required. This would have the same form as for the correction filter for the second stage. In general, a margin of at least 50% between the filter cut-off and wanted channel is recommended to allow for the resistor tolerances and bandwidth change with gain settings noted in section 6.2.2.

As both filter stages are handling large dynamic signals, the linearity of the external capacitors is important. Use of good dielectric materials is recommended; poor linearity could result in a degradation of the on-channel signal in the presence of large off-channel interferers.

#### 6.2.4 Operation at Wider Bandwidths

It is possible to use a much wider channel bandwidth than those used as examples elsewhere in this document. For maximum I/Q bandwidth (1.6 MHz) capacitors C1, C2, C3 and C4 in Figure 9 should be removed. In this case the filter calibration circuit should be disabled using b7 of the VCO Control Register (\$25); see section 7.11.1.

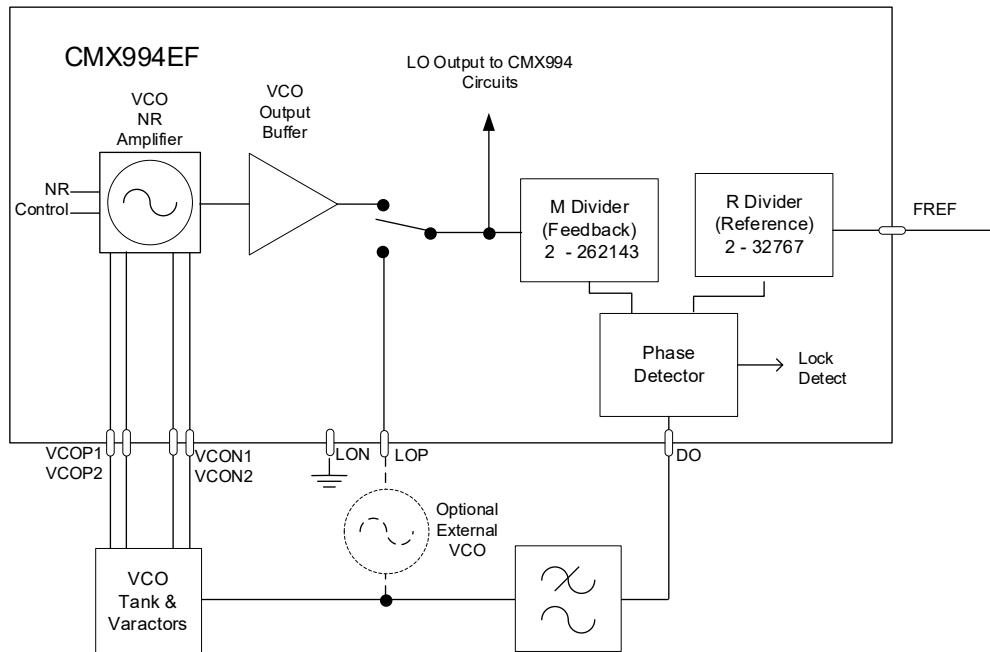
For systems that require greater bandwidths the output should be taken before the baseband amplifiers and filters; see section 8.1.9.

## 6.3 Local Oscillator Operation

The CMX994EF can use either an external Local Oscillator (LO) source or the on-chip VCO and PLL. The on-chip integer-N PLL can also be used with an external VCO connected to the LO input.

### 6.3.1 PLL

The CMX994EF provides an integer-N PLL that can be used to create the local oscillator; see Figure 15. The CMX994EF provides a VCO negative resistance amplifier, so only a tank circuit needs to be implemented externally. Alternatively, this amplifier can be bypassed and an external VCO can be used.



**Figure 15 - Local Oscillator**

The integer-N PLL has programmable M and R dividers as shown in Figure 15. The phase detector provides a charge pump output which requires a suitable loop filter to convert this signal into a control voltage for a VCO. The phase detector can be turned off (high impedance mode) and the PLL section disabled if an external LO is to be used; see section 6.3.2 and 7.9 for control details.

The output frequency of the PLL is set by the following calculation:

$$f_{\text{out}} = f_{\text{ref}} \times (M / R)$$

where:

$f_{\text{out}}$  = The desired output frequency in MHz

$f_{\text{ref}}$  = The reference frequency supplied to the PLL on pin FREF in MHz

M = Divider value programmed in the M divider register (see section 7.9.1)

R = Divider value programmed in the R divider register (see section 7.10.1)

The PLL only supports VCOs with a positive tuning slope, i.e. a higher tuning voltage from DO results in a higher oscillation frequency from the VCO.

The PLL has a lock-detect function that can be evaluated using register \$D2, b6 (section 7.9.2).

The VCO amplifier is a negative resistance amplifier requiring an external tank circuit (see section 5.3.2). The amplifier has two control bits available in the VCO control register (section 7.11.1 register \$25, b2 – b3). These bits can be used to optimise performance for a particular tank circuit depending on its Q value.

When using the CMX994EF PLL, spurious products (spurs) in the receiver I/Q output may be observed. The frequency of the spurs is linked to the PLL M divider value and which of the divide-by-2, 4 or 6 modes is selected for the receiver LO circuits. Operation in divide-by-2 and divide-by-6 modes is most predictable: all even division ratios are problem free and all odd division ratios will give a spurious product at:

$$f_{\text{spur}} = f_{\text{lo}} / ( M * 2 )$$

In divide-by-4 mode most odd divisions will produce a spur although at low frequencies (circa 100 MHz) operation is spur-free. At circa 300 MHz and above some even divisions are also problematic (in divide-by-4 mode).

It is recommended that for safe operation of the CMX994EF PLL, receiver LO divide-by-2 or divide-by-6 modes, with even division ratios, should be used.

When using the CMX994EF PLL, spurious can also be observed in the output from the TXLO pin. In this case the spurs are at small offsets from the wanted signal – the offset is linked to the PLL comparison frequency. The level of these spurs is typically at a very low (< -80 dBc) and less problematic than in the receiver.

### 6.3.2 PLL Enable

The PLL block can be enabled from the General Control Register \$11, b2 (section 7.2.1) and the PLL M Divider Register \$22, b7 (section 7.9.1). An AND function is performed on these two bits (see table below).

| General Control Register \$11, b2 | PLL M Divider Register \$22, b7 | PLL Enable |
|-----------------------------------|---------------------------------|------------|
| 0                                 | 0                               | No         |
| 0                                 | 1                               | No         |
| 1                                 | 0                               | No         |
| 1                                 | 1                               | Yes        |

With the PLL disabled an external local oscillator may be supplied to the CMX994EF.

## 7 C-BUS Interface and Register Descriptions

The C-BUS serial interface supports the transfer of data and control or status information between the CMX994EF's internal registers and an external host. Each C-BUS transaction consists of the host sending a single Register Address byte, which may then be followed by zero or more data bytes that are written into the corresponding CMX994EF register, as illustrated in Figure 16.

Data sent from the host on the Command Data (CDATA) line is clocked into the CMX994EF on the rising edge of the Serial Clock (SCLK) input. The C-BUS interface is compatible with common  $\mu$ C/DSP serial interfaces and may also be easily implemented with general purpose I/O pins controlled by a simple software routine. Section gives the detailed C-BUS timing requirements.

Whether a C-BUS register is of the read or write type, it is fixed for a given C-BUS register address thus one cannot both read and write the same C-BUS register address. The CMX994EF supports several pairs of C-BUS register addresses in order to read and write the same information.

In order to provide ease of addressing when using this device with the CMX998 (Cartesian Feed-back Loop Transmitter IC), the C-BUS addresses below are arranged so as not to overlap those used on the CMX998. Thus, a common chip select (CSN) signal can be used, as well as common CDATA (SDI on CMX998), RDATA (SDO on CMX998) and SCLK signals. Also note that the General Reset (\$10) command on the CMX994EF differs from other CML devices (such as CMX998), which use \$01 for this General Reset function. This allows the CMX994EF and CMX998 to be connected to the same interface pins, including chip select, assuming the drive capabilities of the host are adequate.

### C-BUS Write-only Registers

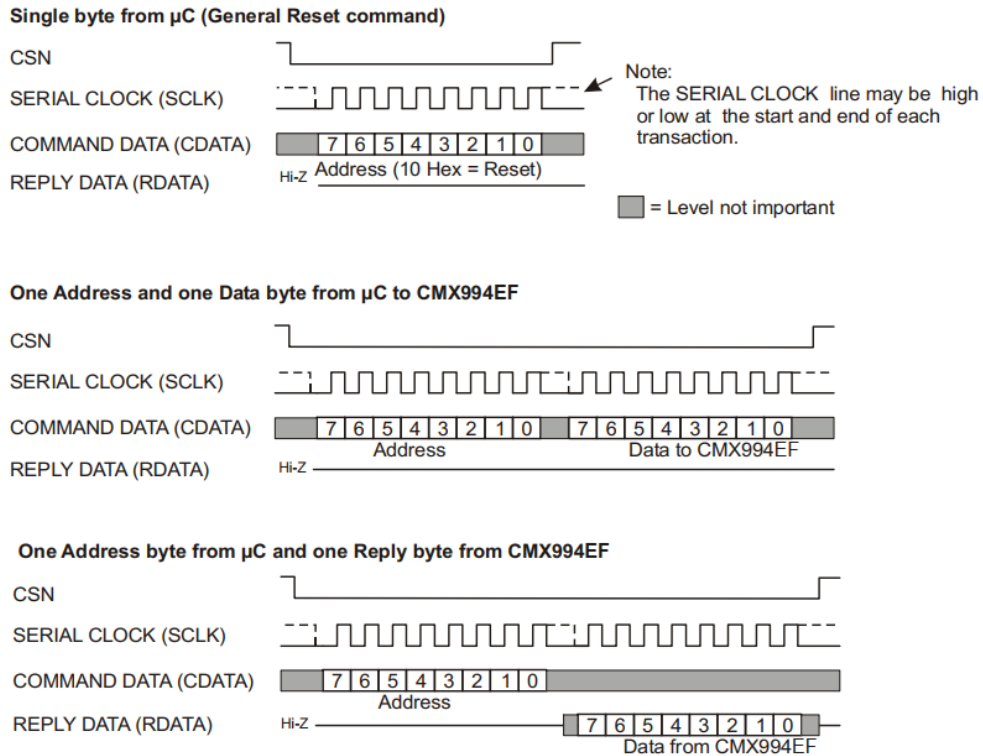
| HEX ADDRESS | REGISTER                                       | WORD SIZE (BITS) |
|-------------|------------------------------------------------|------------------|
| \$10        | General Reset Register (Address only, no data) | 0                |
| \$11        | General Control Register, write only           | 8                |
| \$12        | Rx Control Register, write only                | 8                |
| \$13        | Rx Offset Register, write only                 | 8                |
| \$14        | LNA IM Control Register, write only            | 8                |
| \$15        | Options Control Register, write only           | 8                |
| \$16        | Rx Gain Register, write only                   | 8                |
| \$17        | Extended Rx Offset Register, write only        | 16               |
| \$20-\$22   | PLL M Divider Register, write only             | 8                |
| \$23-\$24   | PLL R Divider Register, write only             | 8                |
| \$25        | VCO Control Register, write only               | 8                |

### C-BUS Read-only Registers

| HEX ADDRESS | REGISTER                               | WORD SIZE (BITS) |
|-------------|----------------------------------------|------------------|
| \$E1        | General Control Register, read only    | 8                |
| \$E2        | Rx Control Register, read only         | 8                |
| \$E3        | Rx Offset Register, read only          | 8                |
| \$E4        | LNA IM Control Register, read only     | 8                |
| \$E5        | Options Control Register, read only    | 8                |
| \$E6        | Rx Gain Register, read only            | 8                |
| \$E7        | Extended Rx Offset Register, read only | 16               |
| \$D0-\$D2   | PLL M Divider Register, read only      | 8                |
| \$D3-\$D4   | PLL R Divider Register, read only      | 8                |
| \$D5        | VCO Control Register, read only        | 8                |

**Notes:**

- All registers will retain data if DVDD and VDDIO pins are held high, even if all other power supply pins are disconnected.
- If clock and data lines are shared with other devices, DVDD and VDDIO must be maintained in their normal operating ranges otherwise ESD protection diodes may cause a problem with loading the signals connected to SCLK, CDATA and RDATA pins, preventing correct programming of other devices. Other supplies may be turned off and all circuits on the device may be powered down without causing this problem.



**Figure 16 - C-BUS Transactions**

**7.1 General Reset: \$10 (no data)**

A command to this register resets the device and clears all bits of all registers. The General Reset command places the device into powersave mode.

Whenever power is applied to the DVDD pin, a built-in power-on-reset circuit ensures that the device powers up into the same state as follows a General Reset command. The RESETN pin on the device will also reset the device to the same state.

## 7.2 General Control Register

### 7.2.1 General Control: \$11 - 8-bit write only

This register controls general features such as powersave. All bits of this register are cleared to '0' by a General Reset command.

| 7       | 6     | 5     | 4  | 3     | 2    | 1    | 0    |
|---------|-------|-------|----|-------|------|------|------|
| En Bias | Freq2 | Freq1 | LP | VCOEN | PLEN | RXEN | TXEN |

b7 and 4-0:

These bits control power up/power down of the various blocks of the IC. In all cases '1' = power up, '0' = power down.

b7 Enables BIAS generator

b4 Enables low power mode. When b4 = '0' the device is operating normally, when b4 = '1' the device will have reduced power consumption and reduced intermodulation performance. See also section 8.1.5 regarding other low power modes.

b3 Enables VCO: When b3 = '1' the setting of the VCO Control Register (\$25) takes effect. For details of VCO Control Register see section 7.11.

b2 PLL Enable: This bit enables the PLL and is ANDed with PLL M-Divider Register (\$22) b7 – section 7.9.1 See also section 6.3.2.

b1 C-BUS Rx Enable; see section 6.1.1

b0 C-BUS Tx Enable; see section 6.1.1

b6, b5

These bits optimise the amplitude of the local oscillator path within the device in order to maintain phase balance and noise performance of the receiver mixers over the full range of operating frequencies.

| b6 | b5 | Operation          |
|----|----|--------------------|
| 0  | 0  | 100 MHz – 150 MHz  |
| 0  | 1  | 150 MHz – 300 MHz  |
| 1  | 0  | 300 MHz – 700 MHz  |
| 1  | 1  | 700 MHz – 1000 MHz |

### 7.2.2 General Control: \$E1 - 8-bit read only

This register reads the value in register \$11; see section 7.2.1 for details of bit functions.

## 7.3 Rx Control Register

### 7.3.1 Rx Control: \$12 – 8-bit write only

This register controls general features of the receiver such as Powersave. All bits of this register are cleared to '0' by a General Reset command.

| 7       | 6      | 5       | 4        | 3        | 2        | 1    | 0    |
|---------|--------|---------|----------|----------|----------|------|------|
| Mix Pwr | IQ Pwr | LNA Pwr | ACR Flt2 | ACR Flt1 | DC Range | DIV2 | DIV1 |

b7-5 These bits control power up/power down of the various blocks of the IC. In all cases '0' = power up, '1' = power down.

|    |                                                   |
|----|---------------------------------------------------|
| b7 | Disable receiver mixers and divider (see note)    |
| b6 | Disable baseband amplifier and filters (see note) |
| b5 | Disable LNA (see note)                            |

Note: These control signals disable the appropriate blocks of the receiver when 'Rx ON' is active. If 'Rx ON' is not active all receiver circuits will be in powersave mode.

b4,3 The baseband I/Q chain provides a narrow filter for rejecting adjacent channel signals. The bandwidth of this filter may be scaled using these bits. For further details see sections 6.2.2, 6.2.3 and 8.1.6.

| b4 | b3 | Function                    |
|----|----|-----------------------------|
| 0  | 0  | Minimum bandwidth           |
| 0  | 1  | Intermediate bandwidth      |
| 1  | 0  | Maximum bandwidth           |
| 1  | 1  | <i>reserved, do not use</i> |

b2 When b2 = '0' the range of DC correction of the I/Q output is nominal (see sections 6.2.1 and 7.4). With b2 = '1' the total correction range is twice the nominal specified in section 7.4 with all steps doubled in value. Note: an alternative method of achieving increased correction range without losing resolution using the Extended Rx Offset Register (\$17); see section 7.8.

b1,0 Receiver LO divider control

| b1 | b0 | Function                    |
|----|----|-----------------------------|
| 0  | 0  | LO divided by 2             |
| 0  | 1  | LO divided by 4             |
| 1  | 0  | LO divided by 6             |
| 1  | 1  | <i>reserved, do not use</i> |

### 7.3.2 Rx Control: \$E2 – 8-bit read only

This read-only register mirrors the value in register \$12; see section 7.3.1 for details of bit functions.

## 7.4 Rx Offset Register

### 7.4.1 Rx Offset: \$13 – 8-bit write only

**Note:** Increased correction range is available by using register \$17; see section 7.8. The bits in registers \$13 and \$17 control the same hardware functions with the most recent write to \$17 or \$13 being applicable at any given time; if \$13 is written then QDC5, QDC4, IDC5 and IDC4 in \$17 are automatically set to '0'. All bits of registers \$13 and \$17 are cleared to '0' by a General Reset command.

| 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|------|------|------|------|------|------|------|------|
| QDC3 | QDC2 | QDC1 | QDC0 | IDC3 | IDC2 | IDC1 | IDC0 |

b7-0 I/Q DC offset correction; see section 6.2.1 for further details. The step size can be doubled using the Rx Control Register (\$12), b2; see section 7.3.1.

The values in the table below are the effects of the offset at the maximum VGA gain (minimum attenuation) setting. They are proportionately lower for lower gain settings (as set by the Rx Gain Register (b2 – b0). The aim of this Rx Offset Register is to allow output offsets to be reduced sufficiently (typically <20 mV) to avoid any significant reduction in the dynamic range of any subsequent ADC. It is expected that demodulation software in the baseband processor would be required to correct for the remaining offset as part of the demodulation process.

See also section 8.1.2.

| b3<br>b7 | b2<br>b6 | b1<br>b5 | b0<br>b4 | I Channel at maximum gain<br>Q Channel at maximum gain |
|----------|----------|----------|----------|--------------------------------------------------------|
| 1        | 1        | 1        | 1        | -140 mV                                                |
| 1        | 1        | 1        | 0        | -120 mV                                                |
| 1        | 1        | 0        | 1        | -100 mV                                                |
| 1        | 1        | 0        | 0        | -80 mV                                                 |
| 1        | 0        | 1        | 1        | -60 mV                                                 |
| 1        | 0        | 1        | 0        | -40 mV                                                 |
| 1        | 0        | 0        | 1        | -20 mV                                                 |
| 1        | 0        | 0        | 0        | No correction                                          |
| 0        | 1        | 1        | 1        | +140 mV                                                |
| 0        | 1        | 1        | 0        | +120 mV                                                |
| 0        | 1        | 0        | 1        | +100 mV                                                |
| 0        | 1        | 0        | 0        | +80 mV                                                 |
| 0        | 0        | 1        | 1        | +60 mV                                                 |
| 0        | 0        | 1        | 0        | +40 mV                                                 |
| 0        | 0        | 0        | 1        | +20 mV                                                 |
| 0        | 0        | 0        | 0        | No correction                                          |

### 7.4.2 Rx Offset: \$E3 - 8-bit Read only

This read-only register mirrors the value in register \$13; see section 7.4.1 for details of bit functions.

## 7.5 LNA Intermodulation Control Register

### 7.5.1 LNA IM Control: \$14 – 8-bit write only

This register controls features of the receiver that support intermodulation optimisation. All bits of this register are cleared to '0' by a General Reset command.

| 7 | 6 | 5   | 4   | 3   | 2   | 1   | 0   |
|---|---|-----|-----|-----|-----|-----|-----|
| 0 | 0 | IM5 | IM4 | IM3 | IM2 | IM1 | IM0 |

b7,6 *reserved*, clear to '0'

b5-0 These bits allow the user to adjust the intermodulation performance of the LNA. The default value is '0' for all the bits. Improved intermodulation can be achieved with a particular value in these bits. For further details see section 8.1.4.

### 7.5.2 LNA IM Control: \$E4 – 8-bit read only

This read-only register mirrors the value in register \$14; see section 7.5.1 for details of bit functions.

## 7.6 Options Control Register

### 7.6.1 Options Control: \$15 – 8-bit write only

All bits of this register are cleared to '0' by a General Reset command.

| 7    | 6   | 5        | 4        | 3   | 2   | 1     | 0     |
|------|-----|----------|----------|-----|-----|-------|-------|
| IP3X | LOX | Reserved | Reserved | PDQ | PDI | PHCON | PHOFF |

- b7 '1' enables enhanced mixer intermodulation mode in the receive path mixers; normal operation when set to '0'.
- b6 When set to '1' enables an alternative LO path bias mode; set to '0' selects normal LO path mode.
- b5 *reserved*, clear to '0'
- b4 *reserved*, clear to '0'
- b3 When set '1' this bit will power down all circuitry in the Q path leaving only the I channel active; normal operation (I and Q paths active) when bit is cleared to '0'.
- b2 When set '1' this bit will power down all circuitry in the I path leaving only the Q channel active; normal operation (I and Q paths active) when bit is cleared to '0'.
- b1-0 LO Phase Correction Control

| b1 | b0 | LO Phase Correction          |
|----|----|------------------------------|
| 0  | 0  | Enabled                      |
| 1  | 1  | Powered down                 |
| 0  | 1  | <i>reserved</i> , do not use |
| 1  | 0  | <i>reserved</i> , do not use |

### 7.6.2 Options Control: \$E5 – 8-bit read only

This register reads the value in register \$15; see section 7.6.1 for details of bit functions.

## 7.7 Rx Gain Register

### 7.7.1 Rx Gain: \$16 – 8-bit write only

This register controls receiver gain control. All bits of this register are cleared to '0' by a General Reset command.

| 7   | 6   | 5         | 4         | 3                  | 2  | 1  | 0  |
|-----|-----|-----------|-----------|--------------------|----|----|----|
| GS1 | GS0 | LNA Gain2 | LNA Gain1 | LNA Z <sub>0</sub> | G2 | G1 | G0 |

b7,6 LNA Gain Control Step: These bits control the LNA gain steps; the nominal step is 6 dB however the actual step size can be adjusted by +0.7 dB, +1.4 dB or +2.8 dB, as shown in the table below. For further information see section 8.1.3.

| b7 | b6 | Function                   |
|----|----|----------------------------|
| 0  | 0  | Nominal step size of 6 dB  |
| 0  | 1  | Nominal step size + 0.7 dB |
| 1  | 0  | Nominal step size+1.4 dB   |
| 1  | 1  | Nominal step size +2.8 dB  |

b5,4 LNA Gain Control: These bits control the LNA gain in nominal 6 dB steps, as shown in table below; see also b7 - b6.

| b5 | b4 | Function                  |
|----|----|---------------------------|
| 0  | 0  | LNA gain = Nominal        |
| 0  | 1  | LNA gain = Nominal -6 dB  |
| 1  | 0  | LNA gain = Nominal -12 dB |
| 1  | 1  | LNA gain = Nominal -18 dB |

b3 Sets the LNA output impedance. The LNA output impedance is approximately 100  $\Omega$  if this bit is set to '0' and approximately 50  $\Omega$  if this bit is set to '1'. If set to 50  $\Omega$  the gain will be increased but with an additional LNA current consumption of approximately 2 mA.

b2-0 I/Q Baseband VGA Control

| b2 | b1 | b0 | VGA Level                 |
|----|----|----|---------------------------|
| 1  | 1  | 1  | VGA = -42 dB              |
| 1  | 1  | 0  | VGA = -36 dB              |
| 1  | 0  | 1  | VGA = -30 dB              |
| 1  | 0  | 0  | VGA = -24 dB              |
| 0  | 1  | 1  | VGA = -18 dB              |
| 0  | 1  | 0  | VGA = -12 dB              |
| 0  | 0  | 1  | VGA = -6 dB               |
| 0  | 0  | 0  | VGA = 0 dB (Maximum gain) |

### 7.7.2 Rx Gain: \$E6 – 8-bit read only

This read only register mirrors the value in register \$16; see section 7.7.1 for details of bit functions.

## 7.8 Extended Rx Offset Register

### 7.8.1 Extended Rx Offset: \$17 – 16-bit write only

All bits of this register are cleared to '0' by a General Reset command.

**Note 1:** the bits in registers \$13 and \$17 control the same hardware functions with the most recent write to \$17 or \$13 being applicable at any given time; if \$13 is written then QDC5, QDC4, IDC5 and IDC4 will automatically be set to '0'.

**Note 2:** QDC3 and IDC3 have different function in \$13 and \$17; in \$13 QDC3 and IDC3 sets the correction polarity whereas in \$17 the polarity is set by QDC5 and IDC5.

|    |    |      |      |      |      |      |      |
|----|----|------|------|------|------|------|------|
| 15 | 14 | 13   | 12   | 11   | 10   | 9    | 8    |
| 0  | 0  | QDC5 | QDC4 | QDC3 | QDC2 | QDC1 | QDC0 |
| 7  | 6  | 5    | 4    | 3    | 2    | 1    | 0    |
| 0  | 0  | IDC5 | IDC4 | IDC3 | IDC2 | IDC1 | IDC0 |

b13-8,

b5-0 I/Q DC Offset correction; see section 6.2.1

The values in the table below are the effects of the offset at the maximum VGA gain (minimum attenuation) setting. They are proportionately lower for lower gain settings (as set by the Rx Gain Register (b2 – b0)). The aim of this Rx Offset Register is to allow output offsets to be reduced sufficiently (typically <20 mV) to avoid any significant reduction in the dynamic range of any subsequent ADC. It is expected that demodulation software in the baseband processor would be required to correct for the remaining offset as part of the demodulation process. See also section 8.1.2

| b5  | b4  | b3  | b2  | b1 | b0 | I Channel at maximum gain<br>Q Channel at maximum gain |
|-----|-----|-----|-----|----|----|--------------------------------------------------------|
| b13 | b12 | b11 | b10 | b9 | b8 |                                                        |
| 1   | 1   | 1   | 1   | 1  | 1  | -620 mV                                                |
| 1   | 1   | 1   | 1   | 1  | 0  | -600 mV                                                |
|     |     |     |     |    |    | etc. (i.e. binary count, step -20 mV)                  |
| 1   | 0   | 0   | 1   | 0  | 1  | -100 mV                                                |
| 1   | 0   | 0   | 1   | 0  | 0  | -80 mV                                                 |
| 1   | 0   | 0   | 0   | 1  | 1  | -60 mV                                                 |
| 1   | 0   | 0   | 0   | 1  | 0  | -40 mV                                                 |
| 1   | 0   | 0   | 0   | 0  | 1  | -20 mV                                                 |
| 1   | 0   | 0   | 0   | 0  | 0  | No correction                                          |
| 0   | 1   | 1   | 1   | 1  | 1  | +620 mV                                                |
| 0   | 1   | 1   | 1   | 1  | 0  | +600 mV                                                |
|     |     |     |     |    |    | etc. (i.e. binary count, step 20 mV)                   |
| 0   | 0   | 0   | 1   | 1  | 1  | +140 mV                                                |
| 0   | 0   | 0   | 1   | 1  | 0  | +120 mV                                                |
| 0   | 0   | 0   | 1   | 0  | 1  | +100 mV                                                |
| 0   | 0   | 0   | 1   | 0  | 0  | +80 mV                                                 |
| 0   | 0   | 0   | 0   | 1  | 1  | +60 mV                                                 |
| 0   | 0   | 0   | 0   | 1  | 0  | +40 mV                                                 |
| 0   | 0   | 0   | 0   | 0  | 1  | +20 mV                                                 |
| 0   | 0   | 0   | 0   | 0  | 0  | No correction                                          |

### 7.8.2 Extended Rx Offset: \$E7 – 16-bit read only

This read-only register mirrors the value in register \$17; see section 7.8.1 for details of bit functions.

## 7.9 PLL M Divider Register

### 7.9.1 PLL M Divider: \$22 - \$20 – 8-bit write only

These registers set the M divider value for the PLL (Feedback Divider). The divider is updated synchronously when register \$22 is written so registers \$20 and \$21 should be written before \$22. Note: the order of writing \$20 and \$21 is not important. Bits 7 and 5 also control the PLL and charge-pump blocks and these control bits are active immediately on any occasion that \$22 is written. (Note: To enable the PLL, b2 of the General Control Register (\$11) must also be used; see section 7.2 See also section 6.3.2.

| \$22 |        |    |   |   |   |     |     | \$21 |     |     |     |     |     |    |    |
|------|--------|----|---|---|---|-----|-----|------|-----|-----|-----|-----|-----|----|----|
| 7    | 6      | 5  | 4 | 3 | 2 | 1   | 0   | 7    | 6   | 5   | 4   | 3   | 2   | 1  | 0  |
| E    | LD_PLL | CP | 1 | 0 | 0 | M17 | M16 | M15  | M14 | M13 | M12 | M11 | M10 | M9 | M8 |

| \$20 |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| M7   | M6 | M5 | M4 | M3 | M2 | M1 | M0 |

**M17-** Phase Locked Loop M divider value

**M0**

**CP** \$22, b5 = '1' enables the charge pump, \$22 b5 = '0' puts the charge pump into high impedance mode

**LD\_PLL** Only write '0' to b6 of \$22 (when read via \$D2, this shows the integer N PLL lock status)

**E** \$22, b7 = '1' enables the PLL; b7 = '0' disables the PLL –This bit enables the PLL and is ANDed with General Control Register (\$11) b2 – section 7.2 See also section 6.3.2

### 7.9.2 PLL M Divider: \$D2-\$D0 - 8-bit read only

These registers read the respective values in registers \$20, \$21 and \$22 (\$D0 reads back \$20 and \$D1 reads back \$21 etc.); see section 7.9.1 for details of bit functions.

Note: \$D2 b6 indicates the Synth lock detect status, b6 = '1' indicates that the PLL is locked, b6 = '0' is the unlocked condition.

## 7.10 PLL R Divider Register

### 7.10.1 PLL R Divider: \$24 - \$23 – 8-bit write only

These registers set the R divider value for the PLL (Reference Divider). The PLL dividers are updated synchronously when \$24 is written. Note: \$23 should be written first then \$24.

| \$24 |     |     |     |     |     |    |    | \$23 |    |    |    |    |    |    |    |
|------|-----|-----|-----|-----|-----|----|----|------|----|----|----|----|----|----|----|
| 7    | 6   | 5   | 4   | 3   | 2   | 1  | 0  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| 0    | R14 | R13 | R12 | R11 | R10 | R9 | R8 | R7   | R6 | R5 | R4 | R3 | R2 | R1 | R0 |

#### R14-R0

Phase Locked Loop R divider value.

**\$24** reserved, set to '0'.

**b7**

### 7.10.2 PLL R Divider: \$D4-\$D3 – 8-bit read only

These registers read the respective values in registers \$23 and \$24 (\$D3 reads back \$23 and \$D4 reads back \$24); see section 7.10.1 for details of bit functions.

## 7.11 VCO Control Register

### 7.11.1 VCO Control: \$25 - 8-bit write only

This register controls the operation of the VCO and LO input. VCO Operation is only enabled when b3 = '1' in the General Control Register (\$11), as detailed in section 7.2 All bits of this register are cleared to '0' by a General Reset command.

Note: it is not recommended that the LO input and the VCO are enabled simultaneously.

| 7        | 6      | 5      | 4              | 3       | 2       | 1            | 0              |
|----------|--------|--------|----------------|---------|---------|--------------|----------------|
| FILT_CAL | TXDIV1 | TXDIV0 | LO Input<br>EN | VCO_NR2 | VCO_NR1 | VCO_NR<br>En | VCO_<br>Buf En |

b7 This bit, if set to '1', will disable the Filter Calibration System. The default value is '0'.

b6,5 These bits control the output division of the Tx LO signal available at pin TXLO. The LO signal is divided by the factor as shown in the following table.

| b6 | b5 | Function    |
|----|----|-------------|
| 0  | 0  | Divide by 2 |
| 0  | 1  | Divide by 4 |
| 1  | 0  | Divide by 6 |
| 1  | 1  | No division |

b4,1,0 These bits control power up/power down of the various blocks of the device  
In all cases, '1' = power up, '0' = power down

|    |                                                                                                                       |
|----|-----------------------------------------------------------------------------------------------------------------------|
| b4 | Enable LO input                                                                                                       |
| b1 | Enable VCO NR Amplifier. When disabled the amplifier is bypassed to support the application of an external LO signal. |
| b0 | Enable VCO Buffer                                                                                                     |

b3,2 VCO amplifier Negative Resistance (NR) control bits optimise phase noise performance. These bits control the Negative Resistance (magnitude of the negative transconductance) of the on-chip VCO NR amplifier. The NR minimum mode would thus be used with the lowest Q external tank circuit and NR maximum with the highest Q value.

| B3 | B2 | Function                |
|----|----|-------------------------|
| 0  | 0  | NR maximum              |
| 0  | 1  | NR intermediate value 1 |
| 1  | 0  | NR intermediate value 2 |
| 1  | 1  | NR minimum              |

**Note:** Performance of CMX994EF with the NR control bits may differ from the earlier versions of the CMX994x family, see also section 5.3.2; the settings 'NR intermediate value 2' and 'NR minimum' are recommended.

### 7.11.2 VCO Control: \$D5 - 8-bit read only

This register reads the value in register \$25; see section 7.11.1 for details of bit functions.

## 8 Application Notes

### 8.1 Typical Receiver Performance

#### 8.1.1 System Performance

This information is intended as a general guide of what can be expected from a CMX994EF receiver design using the on-chip LNA and I/Q down-conversion stages. The measurement circuit uses the component values given in section 5.2 The results are based on measurements from evaluation of the CMX994EF operating at 450 MHz (in normal mode, not enhanced mode). Results are also given for Low Power (LP) mode operation, i.e. General Control Register (\$11) b4 = '1'; see section 7.2.1.

|                                     |                                 |
|-------------------------------------|---------------------------------|
| Gain                                | 63 dB (61.5 dB in LP mode)      |
| Noise Figure:                       | 4.0 dB (also 4.5 dB in LP mode) |
| Input Third Order Intercept Point:  | -2 dBm (-8 dBm in LP mode)      |
| Input Second Order Intercept Point: | 62 dBm (48 dBm in LP mode)      |

Notes:

Common settings: max gain, max filter bandwidth, freq control bits = 300 to 700 MHz, LNA output impedance = 100 Ω, LO at x2 (900 MHz, level -10 dBm), IM Control Register = 0x3F

Gain is measured from RF input (assumed to be 50 Ω source /load) to differential voltage measured at output of I or Q channels.

Second Order Intercept Point is the average of values measured from differential signals on I and Q; measured at 1 MHz offset.

Using the CMX994EF operating at 448 MHz combined with the CMX7164FI-2 modem IC gives the following typical system performance using 19.2 kbps 4-FSK modulation, alpha =0.2, deviation =3 kHz (based on a 25 kHz RF channel).

|                            |                          |
|----------------------------|--------------------------|
| Sensitivity for 1% BER     | -116 dBm (see Figure 17) |
| Blocking                   | >90 dB                   |
| Adjacent channel rejection | 73 dB                    |
| Intermodulation            | 65 dB                    |

(Measurement methods based on EN 300 113).

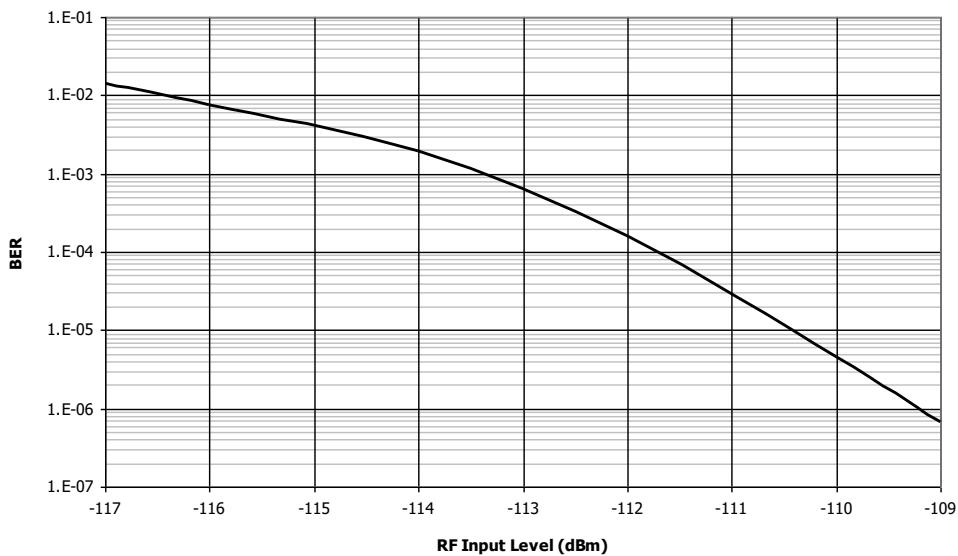


Figure 17 CMX994EF and CMX7164 with FI-2 – Typical 4-FSK Sensitivity (19.2 kbps)

### 8.1.2 DC Offsets

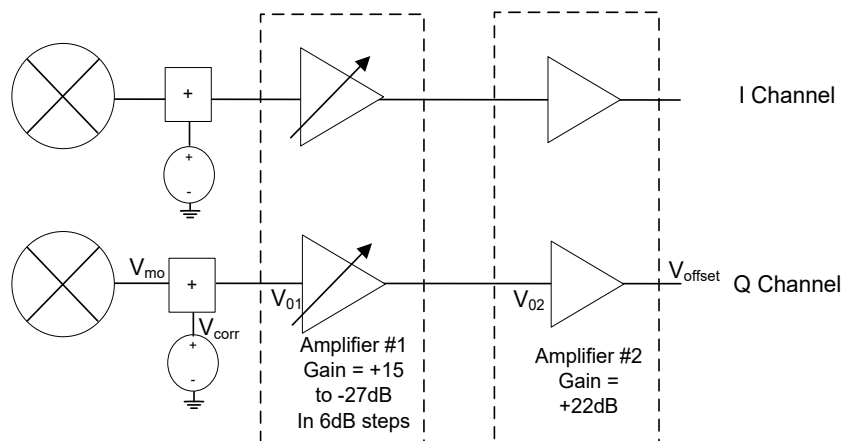
For true direct conversion receiver's dc offsets require careful consideration in the receiver demodulator solution. The CMX994EF has been designed to minimise the dc offset challenges by ensuring excellent mixer IIP2 performance.

For Near Zero IF and low IF receiver systems (see section 8.4) the dc offset issues discussed in the following sub-sections can largely be ignored.

#### 8.1.2.1 Static Offsets

To provide an approximate correction of dc offsets use the following procedure: with the attenuation set at minimum (i.e. max gain) measure the offset at the CMX994EF I or Q output, then the table in section 7.4.1 can be used to give the required offset correction. The range double bit (\$12, b2) can be used to increase the correction range if required. Note that at high attenuation settings there may be an additional error due to residual offsets from within the VGA as explained below.

The dc offsets in the CMX994EF baseband path are shown in Figure 18. The voltages are only shown on the Q path, but the same considerations apply to the I path. Note that the dc offsets in I and Q paths will be different because they relate to random offsets in a number of components; note also that the I and Q paths are differential and that further details of the dc offset correction mechanism are given in section 6.2.1.



Where:

$V_{m0}$  = dc offset at the output of the mixer

$V_{01}$ ,  $V_{02}$  = input offsets of amplifiers 1 and 2 respectively

$V_{corr}$  = correction voltage (value set in Rx Offset register, \$13)

$V_{offset}$  = dc offset present at the output

**Figure 18 - I/Q Path dc Offsets**

Referring to Figure 18, the approximate dc offset for a given gain setting can be calculated as:

$$V_{offset} = (V_{m0} + V_{corr} + V_{01}) \cdot G_1 \cdot G_2 + (V_{02} \cdot G_2)$$

The offset  $V_{02}$  can be estimated by setting the attenuation in Amplifier #1 to -42 dB ( $G_1 = -27$  dB) and then measuring  $V_{offset}$ , thus  $V_{02} = (V_{offset} / G_2)$ . The sum of  $(V_{m0} + V_{01})$  can then be estimated given that the gain setting of  $G_1$  and  $V_{corr}$  are known.

Assuming  $V_{offset}$  is minimised using  $V_{corr}$  at minimum attenuation then increasing the attenuation may result in an increase in  $V_{offset}$ , however the error is typically  $\pm 15$  mV ( $\pm 55$  mV absolute maximum). An example of the variation in dc offsets with gain control is shown in Figure 19.

It should be noted that as the attenuation is increased the steps of the offset correction mechanism reduce as the reciprocal of the attenuation. The result is that at maximum attenuation the offset correction steps are  $25 \text{ mV} \times 10^{(-42/20)} = 0.2 \text{ mV}$ .

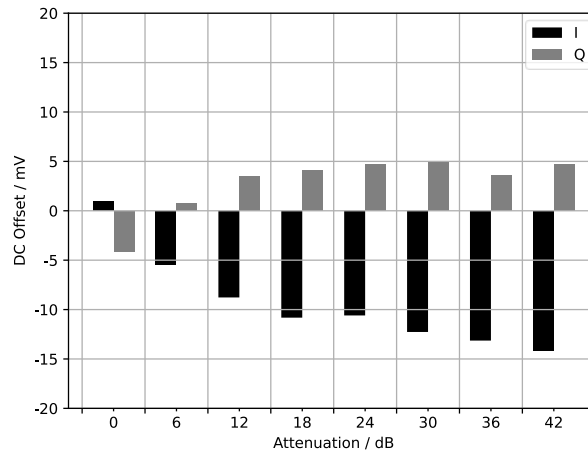


Figure 19 - Example Variation in  $V_{\text{offset}}$  with Gain Control Setting

8.1.2.2 Transient Offsets

The CMX994EF exhibits much improved DC transient performance compared to the previous versions of the CMX994x family, which is advantageous in TDMA systems and will make DC offset tracking much easier.

When a CMX994x family receiver is enabled there is a small variation in the output dc offset resulting from a change in the thermal conditions of the circuit; this is caused by self-heating of the IC. The effect is small, circa 2 mV differential; a typical response is shown in Figure 20. In some radio systems, in particular TDMA systems, the effect may require compensation to avoid an increase in bit errors at the start of reception. The CML DMR modem (product 7341FI-2.x) includes such compensation.

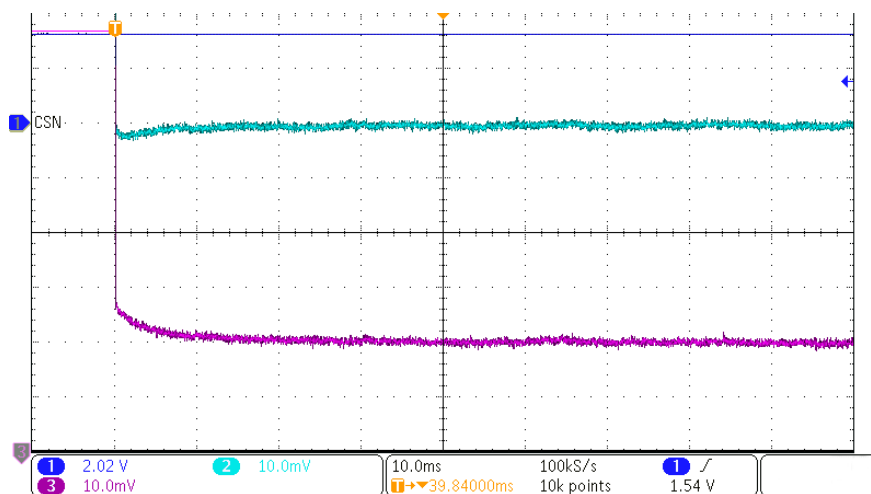
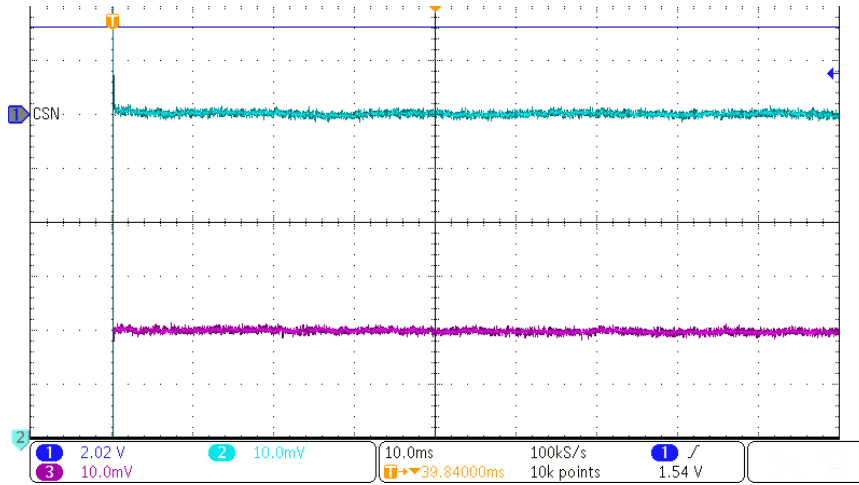


Figure 20 - Typical Transient Response for CMX994EF, Blue trace RXI+ and pink trace = RXQ+, no input signal



**Figure 21- Typical Transient Response for CMX994EF, Blue trace RXI+ and pink trace = RXQ+, no input signal**

In the CMX994EF the transient is much shorter duration (see Figure 22) removing the need for compensation and significantly reducing channel dwell time during scanning.

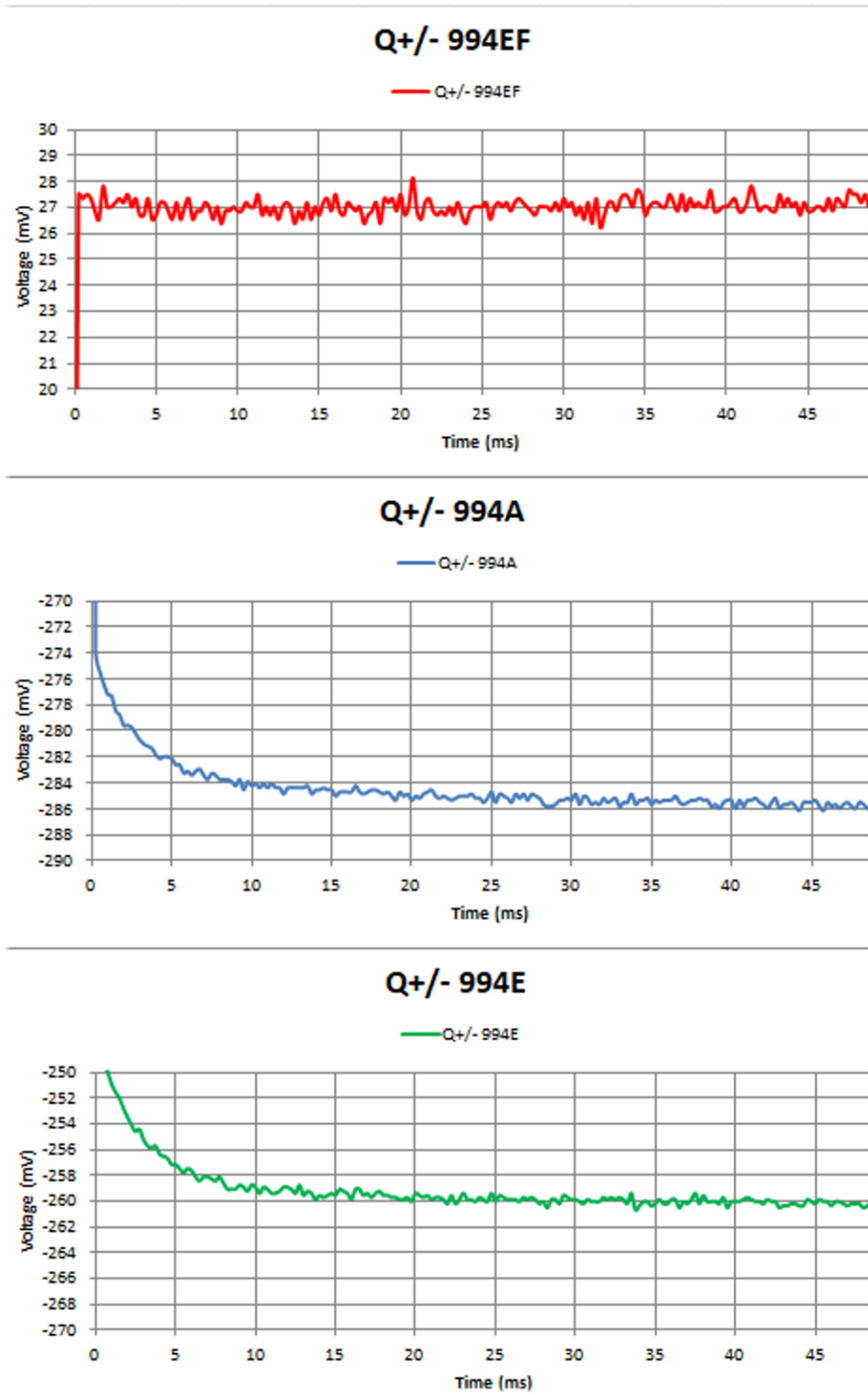


Figure 22 Comparison of Typical Transient Response, Differential Q Channel, no input signal, LO=2 GHz

### 8.1.3 Gain Control

The CMX994EF has gain control mechanisms in the LNA and the baseband (see Figure 23) with a total control range of 60 dB. The gain can be controlled using the Rx Gain Control Register, \$16; see section 7.7.1.

The LNA gain control steps can be adjusted to achieve the required accuracy using the step size control bits in the Rx Gain Control Register. The effect of the step size control varies with frequency, as shown in Table 14 to Table 16. For optimum accuracy the best settings should be selected to suit the particular application. (suggested settings for optimum gain accuracy are shaded grey in the tables.)

The LNA in its 'off' condition (Rx Control Register, \$12, b5='1') can be used as a further step in the LNA control range.

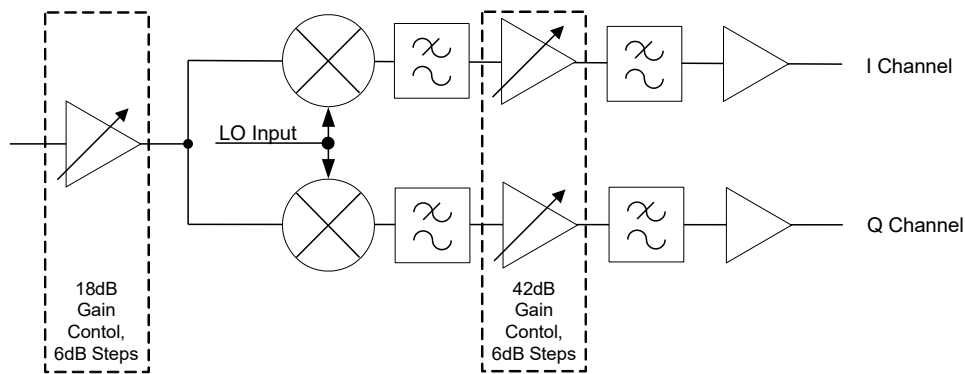


Figure 23 - Gain Control

Table 14 - Typical LNA Gain Step Sizes at 100 MHz,  $Z_o=100\ \Omega$ 

| Gain Setting             | Gain Cntrl Step Size (dB) | Cumulative Gain Change (dB) | Variation from Nominal (dB) |
|--------------------------|---------------------------|-----------------------------|-----------------------------|
| <b>Nominal step size</b> |                           |                             |                             |
| Max                      |                           | 0.0                         |                             |
| -6 dB                    | -7.5                      | -7.5                        | 1.5                         |
| -12 dB                   | -5.6                      | -13.1                       | 1.1                         |
| -18 dB                   | -4.0                      | -17.1                       | 0.9                         |
| <b>Nominal +0.7 dB</b>   |                           |                             |                             |
| Max                      |                           | 0.0                         |                             |
| -6 dB                    | -7.5                      | -7.5                        | 1.5                         |
| -12 dB                   | -6.7                      | -14.27                      | 2.2                         |
| -18 dB                   | -4.0                      | -18.2                       | 0.2                         |
| <b>Nominal +1.4 dB</b>   |                           |                             |                             |
| Max                      |                           | 0.0                         |                             |
| -6 dB                    | -7.6                      | -7.6                        | 1.6                         |
| -12 dB                   | -7.7                      | -15.3                       | 3.3                         |
| -18 dB                   | -3.9                      | -19.2                       | 1.2                         |
| <b>Nominal +2.8 dB</b>   |                           |                             |                             |
| Max                      |                           | 0.0                         |                             |
| -6 dB                    | -7.6                      | -7.6                        | 1.6                         |
| -12 dB                   | -8.8                      | -16.4                       | 4.4                         |
| -18 dB                   | -3.8                      | -20.2                       | 2.2                         |

Table 15 - Typical LNA Gain Step Sizes at 450 MHz,  $Z_o=100 \Omega$ 

| Gain Setting             | Gain Cntrl Step Size (dB) | Cumulative Gain Change (dB) | Variation from Nominal (dB) |
|--------------------------|---------------------------|-----------------------------|-----------------------------|
| <b>Nominal step size</b> |                           |                             |                             |
| Max                      |                           | 0.0                         |                             |
| -6 dB                    | -5.8                      | -5.8                        | 0.2                         |
| -12 dB                   | -4.3                      | -10.1                       | 1.9                         |
| -18 dB                   | -3.1                      | -14.1                       | 4.8                         |
| <b>Nominal +0.7 dB</b>   |                           |                             |                             |
| Max                      |                           | 0.0                         |                             |
| -6 dB                    | -6.2                      | -5.9                        | 0.1                         |
| -12 dB                   | -5.5                      | -11.0                       | 1.0                         |
| -18 dB                   | -3.9                      | -14.1                       | 3.9                         |
| <b>Nominal +1.4 dB</b>   |                           |                             |                             |
| Max                      |                           | 0.0                         |                             |
| -6 dB                    | -5.9                      | -5.9                        | 0.1                         |
| -12 dB                   | -6.0                      | -11.9                       | 0.1                         |
| -18 dB                   | -3.1                      | -14.9                       | 3.1                         |
| <b>Nominal +2.8 dB</b>   |                           |                             |                             |
| Max                      |                           | 0.0                         |                             |
| -6 dB                    | -5.9                      | -5.9                        | 0.1                         |
| -12 dB                   | -6.8                      | -12.7                       | 0.7                         |
| -18 dB                   | -3.1                      | -15.8                       | 2.2                         |

Table 16 - Typical LNA Gain Step Sizes at 900 MHz,  $Z_0=50 \Omega$ 

| Gain Setting             | Gain Cntrl Step Size (dB) | Cumulative Gain Change (dB) | Variation from Nominal (dB) |
|--------------------------|---------------------------|-----------------------------|-----------------------------|
| <b>Nominal step size</b> |                           |                             |                             |
| Max                      |                           | 0.0                         |                             |
| -6 dB                    | -4.9                      | -4.9                        | 1.1                         |
| -12 dB                   | -4.5                      | -9.4                        | 2.6                         |
| -18 dB                   | -3.5                      | -12.9                       | 5.1                         |
| <b>Nominal +0.7 dB</b>   |                           |                             |                             |
| Max                      |                           | 0.0                         |                             |
| -6 dB                    | -4.9                      | -4.9                        | -1.1                        |
| -12 dB                   | -5.5                      | -10.3                       | -1.7                        |
| -18 dB                   | -3.6                      | -13.9                       | -5.1                        |
| <b>Nominal +1.4 dB</b>   |                           |                             |                             |
| Max                      |                           | 0.0                         |                             |
| -6 dB                    | -4.9                      | -4.9                        | 1.1                         |
| -12 dB                   | -6.4                      | -11.3                       | 0.7                         |
| -18 dB                   | -3.7                      | -15.0                       | 3.0                         |
| <b>Nominal +2.8 dB</b>   |                           |                             |                             |
| Max                      |                           | 0.0                         |                             |
| -6 dB                    | -5.0                      | -5.0                        | 1                           |
| -12 dB                   | -7.3                      | -12.3                       | -0.3                        |
| -18 dB                   | -3.8                      | -16.1                       | 1.9                         |

#### 8.1.4 LNA Intermodulation Optimisation

The intermodulation (IMD) performance of the LNA can be optimised using the IM bits in the IM Control register (§14); see section 7.5.1.

For optimum IMD performance is with the IM bits set to maximum, i.e. 0x3F. Typically at 450 MHz for example the improved IMD performance comes with a reduction in gain of approximately 0.5 dB; see Figure 24.

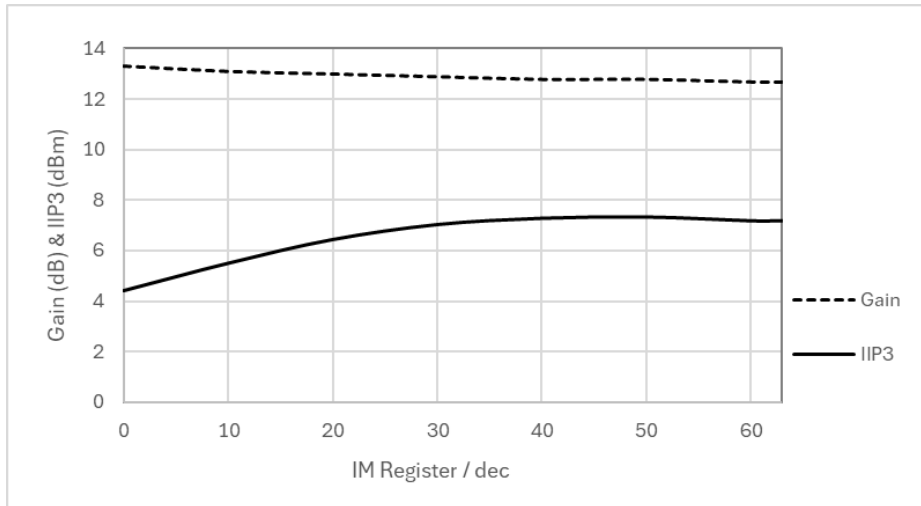


Figure 24 - Variation of LNA Gain and IMD with IM Register Setting, 450 MHz

**8.1.5 Low Power Mode**

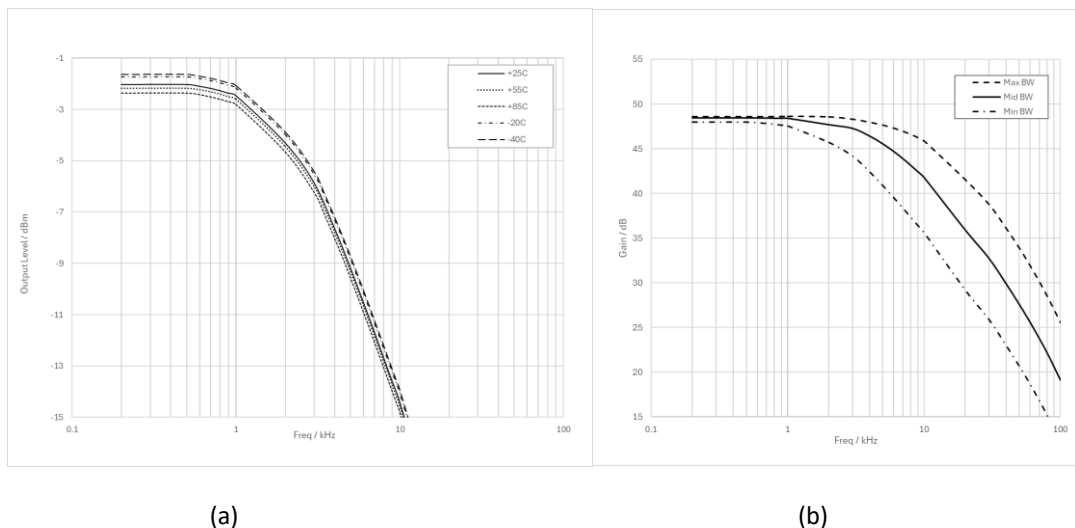
If the low power mode is enabled, General Control Register (\$11) b4 = 1, the total current drawn in the receiver section reduces by approximately 10 mA. For indications of the performance changes in low power mode; see section 8.1.1.

In low power mode at 450 MHz, the degradation in IP2 performance is typically 5 dB. As is usual with IP2 measurements, variations in measured values are observed at different frequency offsets, between I and Q channels and between devices, so average values must be considered.

The CMX994EF has other low power modes that are enabled using the Options Control Register (\$15). Power can be reduced by disabling the phase correction circuits (\$15 = \$03) if the excellent I/Q balance provided by the CMX994EF is not needed. Another option is to disable either I or Q path; this facility is useful for minimising power when monitoring a channel for a RF signal.

**8.1.6 I/Q Filter Response**

The I/Q filter has a well-defined response, and an internal calibration scheme makes it very stable with temperature. The response with temperature, measured for the mixer and baseband path only is shown in Figure 25(a). It will be observed that, apart from a small change in overall gain, the filter response does not vary. The scaling with ACR Flt bits (Rx Control Register (\$12), b4-b3) is shown in Figure 25(b).



(a)

(b)

Figure 25 - I/Q Filter Response

Although the filter calibration circuit gives optimum repeatability and stability over temperature, performance without the calibration is still acceptable in many applications. In such circumstances the filter calibration can be disabled by setting b7 of the VCO control register (\$25) to '1'.

### 8.1.7 LO Pulling

A VCO that uses the on-chip negative resistance amplifier can be pulled in frequency if a high-level signal is applied to the mixer input, as a result of which the VCO becomes modulated resulting in distortion of the output I/Q signals. The level of signal required before the onset of this effect is typically between around -45 dBm and -20 dBm (at the LNA input), depending on the settings of I/Q VGA gain, LNA gain and the PLL.

The LNA gain control provided by the CMX994EF mitigates this effect; at large input signal levels the LNA gain should be set to minimum. Designs using the CMX994EF with an external LNA should consider this issue and ensure the external LNA provides sufficient gain control range.

Designs that use the CMX994EF with an external VCO / PLL, in particular a Fractional-N type, are less susceptible to such frequency pulling but should still employ suitable isolation between the CMX994EF LO input and an external VCO, for example by using a common-base buffer stage.

Following these guidelines a design can readily achieve good receiver system operation with LNA input levels of >+10 dBm.

### 8.1.8 Baseband Intermodulation

The intermodulation (IMD) performance of the CMX994EF I/Q baseband amplifiers is designed to be good enough to ensure that the overall IMD performance of the down-converter section is dominated by the performance of the mixers. Typical in-band linearity with a very large output signal is >80 dBc. Care should be taken in the CMX994EF receiver system design to ensure that the baseband sections do not clip in the presence of intermodulation test signals because, if clipping occurs, the overall intermodulation performance of the receiver will be degraded. The CMX994EF provides two I/Q baseband filter stages which can be used to provide selectivity in order to keep IMD test signals within the receiver dynamic range.

### 8.1.9 Rx Mixer Output (Broadband Operation)

The CMX994EF Rx mixer can be used by coupling the signal from pins IFLT1N, IFLT1P (differential signal, I channel) and QFLT1N, QFLT1P (differential signal, Q channel); see Figure 26. For optimum performance, differential connection is recommended but a single ended connection will also work. The signal is dc coupled with a bias voltage of typically 1.25 V. The typical source impedance of each pin is 800  $\Omega$ . When using this configuration the following recommendations should be followed:

- Components C1, C2, C3, C4 and R1, as shown in Figure 9 are not required;
- If signals are to be coupled from the CMX994EF mixer outputs then the baseband gain must be set to maximum attenuation (-42 dB, minimum gain) by setting all of b2, b1 and b0 of Rx Gain Register: C-BUS address \$16 to a value of '1'; this applies where the baseband sections are enabled or disabled;
- If the baseband sections are enabled (set b6 of Rx Control Register: C-BUS address \$12, to '0') dc offset correction registers may be used to change the dc offset at mixer outputs;
- Capacitance, including stray capacitance in the PCB layout, must be minimised to achieve the maximum available signal bandwidth.

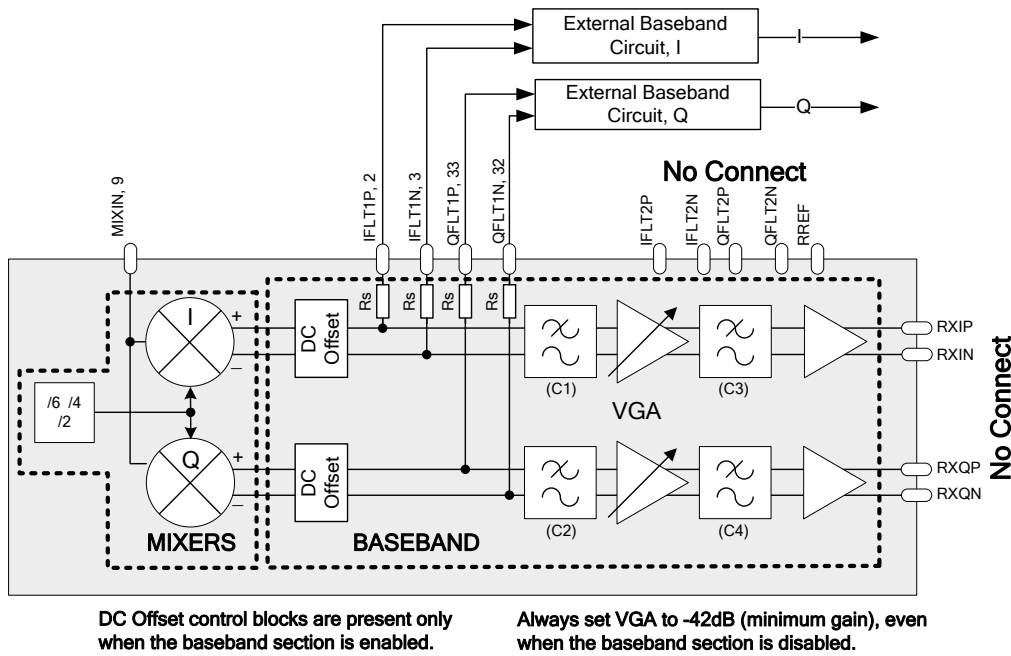


Figure 26 External Baseband Circuit Connections to Mixer

8.1.10 Power Saving Modes

The CMX994EF provides several options which can be used to tailor the power / performance of the device. The host can control this based on a range of parameters so, for example, power can be saved during monitoring of a channel. In the channel monitoring scenario, it may be possible to save power by disabling the I or Q channel. The values in Table 17 show the typical variation in measured values for one CMX994EF device, note operating characteristics are specified in section 9.1.3.

Table 17 - Typical Current Consumption in Various Modes

| Mode                                  | Phase Correction "OFF" | Phase Correction "ON" |
|---------------------------------------|------------------------|-----------------------|
| Enhanced mode                         | 58 mA                  | 72 mA                 |
| Normal operation                      | 49 mA                  | 64 mA                 |
| Low power mode                        | 39 mA                  | 54 mA                 |
| Low power mode and I or Q channel off | 30 mA                  | 40 mA                 |

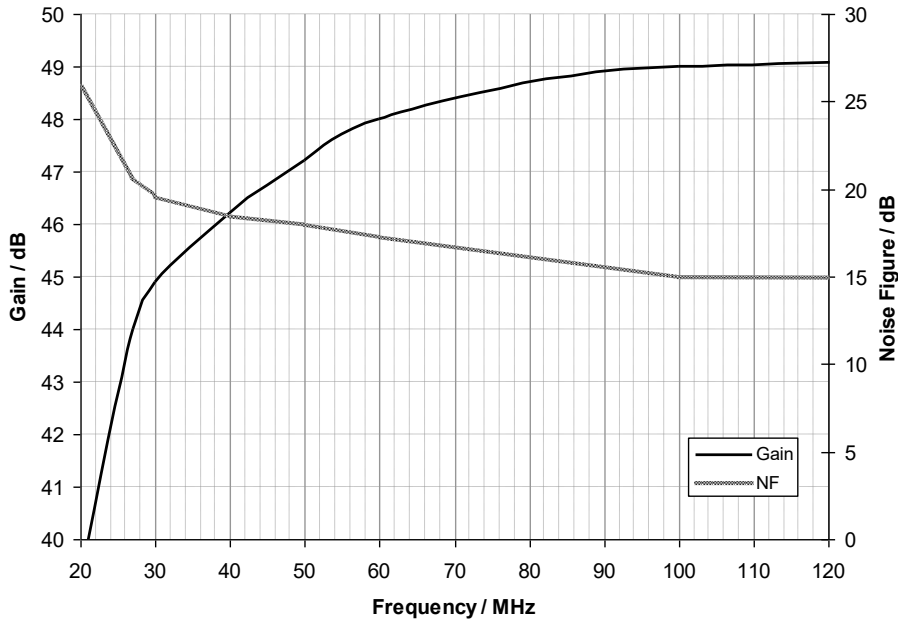
8.1.11 Spurious Responses

An advantage of the direct conversion receiver approach is the inherently low number of spurious responses, however the circuit still has responses at harmonics and sub-harmonics. The circuit designer will need to provide suitable high-pass and low-pass filtering at the CMX994EF input (and/or between LNA and mixers) to prevent such responses.

Note: large signals at sub-harmonic frequencies will generate harmonics in the LNA output which cannot be removed after the LNA because they are on the wanted frequency of the receiver.

### 8.2 Operation Below 100 MHz

The CMX994EF can be safely used below 100 MHz, down to at least 30 MHz, however performance will degrade at lower frequencies and will fall particularly rapidly below 50 MHz.



**Figure 27 - Typical Gain and NF Variation of Demodulator Stages at Low Frequencies**

The LNA can be matched for 30 MHz giving a gain of 15.5 dB and noise figure of 5 dB. Intermodulation is typically +3.5 dBm.

For a 50 MHz application, typical circuit values are shown in Table 18 using the circuit of Figure 7. Typical results using this configuration are shown in Table 19.

**Table 18 – 50 MHz LNA and Inter-stage Components (100 Ω mode)**

|    |               |    |                   |
|----|---------------|----|-------------------|
| C1 | 1nF           | L1 | 560 nH            |
| C2 | 33 pF // 10nF | L2 | 12 pF (capacitor) |
| C3 | 1nF           | L3 | Not Fitted        |

**Table 19 - Summary of Results for the Complete Rx Chain at 50 MHz**

| Parameter    | Result |
|--------------|--------|
| Gain         | 63 dB  |
| Noise Figure | 5 dB   |
| IIP3         | -1 dBm |

### 8.3 Transmitter LO Output

The transmitter LO output is taken from the CMX994EF LO source and is independently buffered or divided to the TXLO pin. The division ratio is selected with the TXDIV0 and TXDIV1 bits in the VCO Control register (\$25, b5-b6; see section 7.11.1). The output level variation with frequency of the TXLO output is shown in Figure 28 and typical variation with temperature is shown in Figure 29.

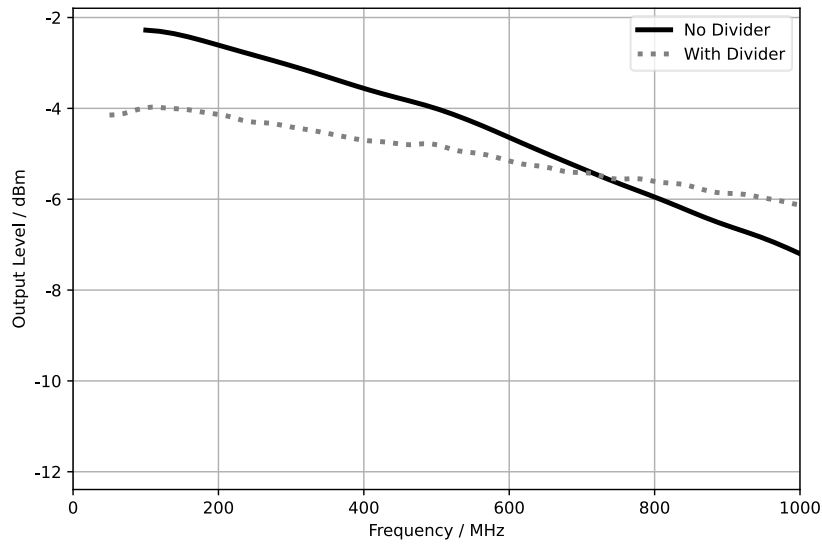


Figure 28 - Tx Output Level vs. Frequency

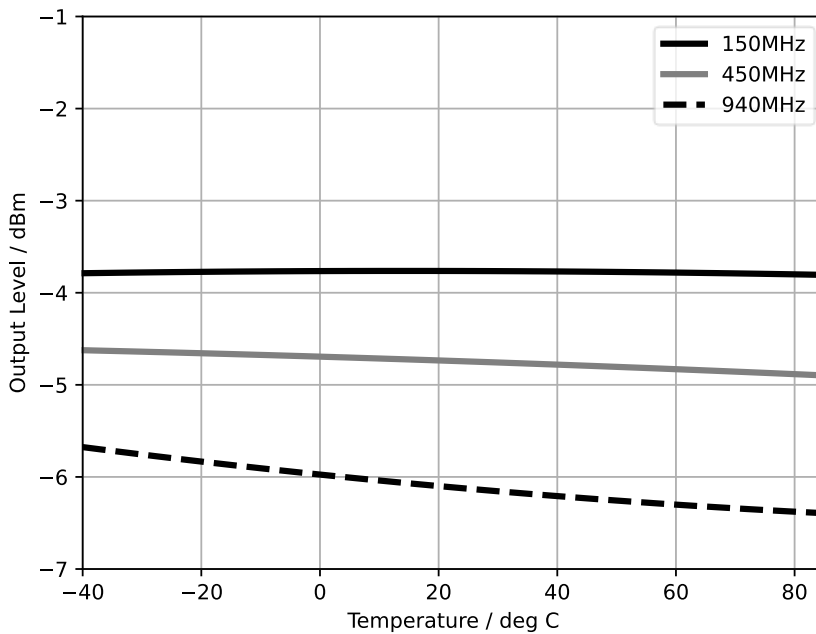


Figure 29 - Typical Tx Output Level (With Divider) vs. Temperature

## 8.4 Modem Solutions

The CMX994EF supports a wide range of modulations. By way of example, the device can be operated with CML baseband / modem devices as shown in Table 20. This table is not exhaustive, and other combinations are also possible.

| Modulation               | Standard                          | CML Modem IC                         | CML Baseband Interface IC |
|--------------------------|-----------------------------------|--------------------------------------|---------------------------|
| 4-FSK                    | dPMR<br>TS 102 490<br>TS 102 658  | CMX7341 (FI-1)<br>CMX7141 (FI-7)     |                           |
| 4-FSK                    | DMR<br>TS 102 361                 | CMX7341 (FI-2)<br>CMX7161            | CMX983                    |
| 4-FSK, 8-FSK, 16-FSK     | General Purpose                   | CMX7164/7364 (FI-2)                  |                           |
| GMSK/GFSK                | General Purpose                   | CMX7164/7364 (FI-1)                  |                           |
| 4-QAM, 16-QAM,<br>64-QAM | General Purpose                   | CMX7163<br>CMX7164/7364 (FI-4)       |                           |
| Pi/4-DQPSK               | TETRA<br>EN 300 392-2             |                                      | CMX983                    |
| C4FM / H-CPM             | APCO P25                          | CMX7341 (FI-4)                       | CMX983                    |
| Analogue FM              | TIA-603, EN 300 296<br>EN 300 086 | CMX7141 (FI-8)<br>CMX7341 (FI-1,3,4) |                           |

**Table 20 - Modulation/Modem Combinations**

## 8.5 Zero IF, near-zero IF and low IF I/Q architectures

The CMX994EF provides a complete receiver signal path including LNA, RF down mixer stage and baseband amplifiers with filters to down convert the wanted RF signal to I/Q baseband while supporting high performance in a small total size. This single conversion approach provides many benefits, e.g. it requires only one LO source, which reduces circuitry and eliminates a source of many spurious responses and relative to multi-stage architectures such as dual superhet, it eliminates one or more bulky image rejection filters. The I/Q output format supports any modulation, including phase coherent constant envelope (e.g. CP-FSK) and linear (QAM) ones.

Mixing the wanted signal down to 0Hz (zero IF) by setting mixer LO and wanted RF signal frequencies to be the same provides a unique benefit, which is that it avoids placing the image of adjacent channel and other close-in interferers at the same frequency band as the wanted modulation. This is especially helpful if one considers that the adjacent channel interferer power may be far greater than the wanted signal's. The zero IF approach also minimises the bandwidth of I/Q output signals, which reduces the cost, power and complexity of ADCs used to sample them. Lastly, it enables a low pass filter on each of I and Q signal paths to provide selectivity, which simplifies design by reducing filter complexity and the required dynamic range of the ADCs. While it is true that second order mixer intermodulation products also lie at 0Hz (DC), the CMX994EF features best in class, (+79 dBm) mixer IIP2 performance to attenuate such DC intermod products.

For specific radio systems one may wish to avoid mixing the wanted signal down to 0Hz. The CMX994EF readily supports this by allowing the user to select LO frequencies that do not exactly match the wanted RF signal's carrier.

Near-zero IF I/Q architectures often set the LO frequency to between half to two times the required channel bandwidth, which provides frequency separation between the wanted signal and any DC components in the output I and Q signals. Such architectures then sample (ADC convert) the near-zero I/Q IF signal pair and then use digital baseband processing to both implement a simple high pass filter that removes DC and perform a final frequency mix down to 0 Hz. Operating in such a near-zero IF mode requires the CMX994EF baseband low pass filters to be scaled wider appropriately to pass the chosen IF frequency; the filter components

external to the CMX994EF will need to be revised; see section 6.2.3. Sampling ADC bandwidth must also be somewhat higher performance and therefore higher power than ADCs used in the zero IF architecture. Another and perhaps more significant trade-off of near-zero IF is that the adjacent channel image generated by unavoidable I/Q gain and phase errors typically now falls on the wanted signal to create a significant interference component if the adjacent channel signal level is high.

The low IF I/Q architecture is a conceptual extension of near-zero IF; it sets the mixer LO frequency to something different than the wanted RF carrier frequency but with even more frequency separation than near-zero IF uses. The result is that the wanted signal is mixed to an even higher frequency at the I/Q outputs. This approach can permit receiver I/Q outputs to be AC coupled to ADCs. Low IF I/Q trade-offs are of the same type as those presented by near-zero IF but they are more challenging, i.e. wider bandwidth ADCs must be used.

The CMX994EF supports all of zero IF, near-zero IF and low IF I/Q architectures, with the benefits of LNA to I/Q output integration with amplification, low pass filtering, and operating modes selected via serial host control.

## 9 Performance Specification

### 9.1 Electrical Performance

For a definition of voltage and reference signals, see section 4.1.

#### 9.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.



**ESD Warning:** This high-performance RF integrated circuit is an ESD sensitive device which has unprotected inputs and outputs. Handling and assembly of this device should only be carried out at an ESD protected workstation.

|                                                                                          | Min. | Max.            | Units |
|------------------------------------------------------------------------------------------|------|-----------------|-------|
| Supply ( $AV_{DD} - AV_{SS}$ ) or ( $DV_{DD} - DV_{SS}$ )                                | -0.3 | +4.0            | V     |
| Voltage on any pin to AGND or DGND pins                                                  | -0.3 | $V_{max} + 0.3$ | V     |
| Voltage between $AV_{DD}$ and $DV_{DD}$                                                  | -0.3 | +0.3            | V     |
| Voltage between AGND and DGND pins                                                       | -50  | +50             | mV    |
| Current into or out of DGND, VDDIO, VCCRXIF, VCCRF, VCCLNA, VCCSYNTH, VCCLO or DVDD pins | -75  | +75             | mA    |
| Current into or out of AGND (exposed metal pad)                                          | -200 | +200            | mA    |
| Current into or out of any other pin                                                     | -20  | +20             | mA    |

Note: see section 4.1 for definitions of signals.

| Q4 Package                                                          | Min. | Max. | Units                  |
|---------------------------------------------------------------------|------|------|------------------------|
| Total Allowable Power Dissipation at $T_{AMB} = 25^{\circ}\text{C}$ | –    | 1820 | mW                     |
| ... De-rating                                                       | –    | 18.2 | mW/ $^{\circ}\text{C}$ |
| Storage Temperature                                                 | -55  | +125 | $^{\circ}\text{C}$     |
| Operating Temperature                                               | -40  | +85  | $^{\circ}\text{C}$     |

#### 9.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

|                                       | Notes | Min. | Max.            | Units              |
|---------------------------------------|-------|------|-----------------|--------------------|
| Analogue Supply ( $AV_{DD}$ )         |       | 3.0  | 3.6             | V                  |
| Digital Supply ( $DV_{DD}$ )          |       | 3.0  | 3.6             | V                  |
| IO Supply ( $VDD_{IO}$ )              |       | 1.6  | $DV_{DD} + 0.3$ | V                  |
| Operating Temperature                 |       | -40  | +85             | $^{\circ}\text{C}$ |
| Maximum continuous input to pin LNAIN | A     |      | +3              | dBm                |

Notes: A. For signals that are not continuous, higher input powers are permitted; power levels above +10 dBm should be avoided especially when the device is operating close to the maximum rated operating temperature.

### 9.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

$AV_{DD} = DV_{DD} = VDD_{IO} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{SS} = AV_{SS} = DV_{SS}$ ,  $T_{AMB} = +25\text{ }^{\circ}\text{C}$ ; registers in default condition except where otherwise specified or as necessary to enable the relevant sections of the device for half duplex operation.

#### DC parameters

| DC Parameters                                                             | Notes | Min. | Typ. | Max. | Units         |
|---------------------------------------------------------------------------|-------|------|------|------|---------------|
| Total Current Consumption                                                 |       |      |      |      |               |
| Powersave Mode                                                            | 1, 2  | –    | 25   | 90   | $\mu\text{A}$ |
| $V_{BIAS}$ Only                                                           | 4     | –    | 1.7  | 3.5  | $\text{mA}$   |
| Operating Currents                                                        |       |      |      |      |               |
| Rx Only                                                                   | 5     | –    | 66   | 80   | $\text{mA}$   |
| Rx Only, Low Power Mode                                                   | 5a    | –    | 56   | –    | $\text{mA}$   |
| Rx Only, Low Power Mode and Phase Correction off                          | 5c    |      | 42   |      | $\text{mA}$   |
| Rx Only, Low Power Mode and Phase Correction off, I or Q channel disabled | 5d    |      | 33   |      | $\text{mA}$   |
| Rx Only, Enhanced Intermodulation Mode                                    | 5e    |      | 74   | 90   | $\text{mA}$   |
| Tx Only                                                                   | 5     | –    | 22   | 30   | $\text{mA}$   |
| Stage currents                                                            |       |      |      |      |               |
| LNA Only                                                                  | 5     | –    | 9    | 15   | $\text{mA}$   |
| LNA in $50\Omega$ Output Mode                                             | 5b    | –    | 11   | –    | $\text{mA}$   |
| I/Q Demodulator                                                           | 5     | –    | 41   | 53   | $\text{mA}$   |
| Baseband I/Q                                                              | 5     | –    | 13   | 15   | $\text{mA}$   |
| VCO and Buffer                                                            | 5     | –    | 10   | 13   | $\text{mA}$   |
| LO Input                                                                  | 5     | –    | 5    | 7    | $\text{mA}$   |
| PLL                                                                       | 5     | –    | 5.5  | –    | $\text{mA}$   |
| Current from $VDD_{IO}$                                                   | 3     | –    | –    | 600  | $\mu\text{A}$ |
| Logic ‘1’ Input Level                                                     |       | 70%  | –    | –    | $VDD_{IO}$    |
| Logic ‘0’ Input Level                                                     |       | –    | –    | 30%  | $VDD_{IO}$    |
| Output Logic ‘1’ Level ( $I_{OH} = 0.6\text{ mA}$ )                       |       | 80%  | –    | –    | $VDD_{IO}$    |
| Output Logic ‘0’ Level ( $I_{OL} = -1.0\text{ mA}$ )                      |       | –    | –    | +0.4 | $\text{V}$    |
| Power-up Time                                                             |       |      |      |      |               |
| Internal Bias Supplies                                                    | 6, 7  | –    | –    | 0.5  | $\text{ms}$   |
| All Blocks Except Internal Bias                                           | 6     | –    | –    | 10   | $\mu\text{s}$ |

- Notes:
1. Powersave mode current applies to both the following operating cases: (a) after a General Reset command has been issued and with all analogue and digital supplies applied and also (b) with DV<sub>DD</sub> applied but with all analogue supplies disconnected. For case (b), DV<sub>DD</sub> current will not exceed the specified value and is independent of the state of the registers.
  2. T<sub>AMB</sub> = 25°C, not including any current drawn from the device pins by external circuitry.
  3. Assumes 30pF on each C-BUS interface line and an operating serial clock frequency of 5 MHz.
  4. The stated current drawn here is with the bandgap reference and accompanying bias current generators enabled only (General Control Register – \$11), all other circuitry is disabled.
  5. Not including any current drawn from the device pins by external circuitry or the bias current.  
Rx Only – Rx Circuitry as enabled: Rx Gain Register = 0x00, General Control Register = 0xC2, Rx Control Register = 0x10 and Intermodulation Control Register = 0x3F;  
TX Only – General Control Register = 0x81, divide by 2 mode;  
LNA Only – 0x82 is written to the General Control Register and 0xC0 to the Rx Control register;  
I/Q Demodulator – 0x60 is written to the Rx Control register;  
Baseband I/Q – 0xA0 is written to the Rx Control register;  
VCO and Buffer – 0x88 is written to the General Control Register and 0x03 to the VCO Control Register;  
LO Input – 0x84 is written to the General Control Register and 0x10 to the VCO Control Register;  
PLL – 0x00 is written to the VCO Control Register, 0x82 is written to the General Control Register and 0x80 to PLL M register (\$22).
    - 5a. As note 5 except General Control Register (\$11) b4 = '1'; see sections 7.2.1 and 8.1.5.
    - 5b. As note 5 except Rx Gain Register (\$16) b3 = '1'; see section 7.7.1.
    - 5c. As note 5 except General Control Register (\$11) b4 = '1'; see section 7.2.1, Option Control Register (\$15) b0 = '1' and b1 = '1'; see section 7.6.1.
    - 5d. As note 5 except General Control Register (\$11) b4 = '1'; see section 6.2.1, Option Control Register (\$15) b3- b0 = '1011 or '0111' section 6.6.1.
    - 5e. As note 5 except Option Control Register (\$15) b8 = '1'; see section 7.6.1
  6. As measured from the rising edge of CSN.
  7. Bias is enabled by General Control Register (\$11) b7; see section 7.2.1
  8. Not used
  9. Not used

**AC Parameters – Low Noise Amplifier Section**

| LNA                                 | Notes  | Min. | Typ.           | Max. | Units    |
|-------------------------------------|--------|------|----------------|------|----------|
| Gain                                |        |      |                |      |          |
| 100 MHz                             | 14     | –    | 15             | –    | dB       |
| 450 MHz                             | 12,14  | –    | 12.5           | –    | dB       |
| 1000 MHz                            | 17     | –    | 12             | –    | dB       |
| Reverse Isolation ( $S_{12}$ )      |        |      |                |      |          |
| 100 MHz                             | 14     | –    | -40            | –    | dB       |
| 450 MHz                             | 14     | –    | -25            | –    | dB       |
| 1000 MHz                            | 17     | –    | -22            | –    | dB       |
| Gain Control Range                  | 16     | –    | 18             | –    | dB       |
| Gain Control Step Size              | 16     | 4    | 6              | 8    | dB       |
| Change in Gain with LNA off         |        |      |                |      |          |
| 450 MHz                             | 19     | -30  | -36            | –    | dB       |
| 1000 MHz                            | 19     | -20  | -25            | –    | dB       |
| Noise Figure                        |        |      |                |      |          |
| 100 MHz                             | 14     | –    | 2              | –    | dB       |
| 450 MHz                             | 14     | –    | 2              | –    | dB       |
| 1000 MHz                            | 17     | –    | 2.5            | –    | dB       |
| Third Order Intercept Point (input) |        |      |                |      |          |
| 100 MHz                             | 14     | –    | 8              | –    | dBm      |
| 450 MHz                             | 11,14  | –    | 5.5            | –    | dBm      |
| 1000 MHz                            | 11,17  | –    | 6              | –    | dBm      |
| 1dB Gain Compression Point (input)  |        |      |                |      |          |
| 100 MHz                             | 14     | –    | -12            | –    | dBm      |
| 450 MHz                             | 14     | –    | -12            | –    | dBm      |
| 1000 MHz                            | 17     | –    | -11            | –    | dBm      |
| Input Impedance                     | 10     | –    | –              | –    | $\Omega$ |
| Output Impedance (100R mode)        | 10, 13 | –    | 100R //<br>1pF | –    | $\Omega$ |
| Operating Frequency Range           | 15     | 100  | –              | 1000 | MHz      |
| LO Leakage at LNA Input             |        | –    | <-90           | –    | dBm      |

- Notes:
10. For further details see section 5.2.1
  11. Intermodulation optimised using Intermodulation Control Register, for further details see section 6.5.
  12. The gain is approximately 2 dB higher if the LNA  $Z_0$  (Rx Gain Register b3) is set to '1'.
  13. The impedance is approximately 50  $\Omega$  if the LNA  $Z_0$  (Rx Gain Register b3) is set to '1'.
  14. Measured at maximum gain with the LNA  $Z_0$  (Rx Gain Register b3) set to '0' and IM reg = 63hex. LNA matched for stated frequency.
  15. For extended operation down to 50 MHz see section 8.2.
  16. See section 8.1.3 for further details
  17. LNA  $Z_0$  = 50  $\Omega$  (Rx Gain Register b3 set to '1') and IM reg = 63hex. LNA matched for stated frequency.
  18. LNA off with Rx Control Register ( $S_{12}$ ) b5 set to '1'.
  19. Change relative to LNA on state, change in gain measured at baseband to account for impedance changes between on and off states; input signal level -45 dBm.

**AC Parameters – Direct Conversion Receiver Sections (in normal mixer intermod mode)**

| <b>I/Q Demodulator<br/>(combined performance of receiver sections,<br/>excluding LNA)</b> | <b>Notes</b> | <b>Min.</b> | <b>Typ.</b> | <b>Max.</b> | <b>Units</b> |
|-------------------------------------------------------------------------------------------|--------------|-------------|-------------|-------------|--------------|
| Gain                                                                                      |              |             |             |             |              |
| 450 MHz                                                                                   |              | –           | 49          | –           | dB(V/V)      |
| 1000 MHz                                                                                  |              | –           | 49          | –           | dB(V/V)      |
| Noise Figure                                                                              |              |             |             |             |              |
| 450 MHz                                                                                   |              | –           | 14.5        | –           | dB           |
| 1000MHz                                                                                   |              | –           | 17          | –           | dB           |
| Third Order Intercept Point (Input)                                                       |              |             |             |             |              |
| 450 MHz                                                                                   |              | –           | 11          | –           | dBm          |
| 1000 MHz                                                                                  |              | –           | 10          | –           | dBm          |
| Second Order Intercept Point (Input)                                                      |              |             |             |             |              |
| 100 MHz to 600 MHz                                                                        | 25           | –           | 79          | –           | dBm          |
| 600 MHz to 1000 MHz                                                                       | 25a          | –           | 70          | –           | dBm          |
| 1dB Compression Point (Input)                                                             | 24, 24a      | –           | 0           | –           | dBm          |
| Image Rejection (I/Q Gain/Phase Matching)                                                 |              |             |             |             |              |
| LO Phase Correction On                                                                    |              | 30          | 40          | –           | dB           |
| LO Phase Correction Off                                                                   | 24           | 25          | –           | –           | dB           |
| I/Q Amplitude Balance                                                                     |              |             |             |             |              |
| LO Phase Correction On                                                                    |              | –           | ± 0.03      | ± 0.2       | dB           |
| LO Phase Correction Off                                                                   | 24           | –           | ± 0.1       | –           | dB           |
| I/Q Phase Balance                                                                         |              |             |             |             |              |
| LO Phase Correction On                                                                    |              | –           | ± 0.5       | ± 2.0       | deg.         |
| LO Phase Correction Off                                                                   | 24           | –           | ± 1         | ± 3         | deg.         |
| I/Q DC Offset Correction Steps                                                            | 22           | 12          | 20          | 28          | mV           |
| I/Q DC Offset at Maximum Attenuation                                                      | 20a          | –           | ±15         | ±55         | mV           |
| I/Q Output Bandwidth                                                                      | 23           | –           | –           | 1.6         | MHz          |
| LO Divider Ratios (selectable)                                                            |              | –           | 2, 4 or 6   | –           |              |
| I/Q Differential Output Voltage Swing                                                     | 20           | –           | –           | 4.0         | Vp-p         |
| Blocking                                                                                  | 21           | 93          | 96          | –           | dB           |

**AC Parameters – Direct Conversion Receiver Sections (register \$15, b7 set to '1' (enhanced mixer intermodulation mode))**

| I/Q Demodulator<br>(combined performance of receiver sections, excluding LNA) | Notes   | Min. | Typ.      | Max.  | Units   |
|-------------------------------------------------------------------------------|---------|------|-----------|-------|---------|
| Gain                                                                          |         |      |           |       |         |
| 450 MHz                                                                       |         | –    | 49        | 52    | dB(V/V) |
| 1000 MHz                                                                      |         | –    | 49        | 52    | dB(V/V) |
| Noise Figure                                                                  |         |      |           |       |         |
| 100 MHz                                                                       |         | –    | 14.5      | –     | dB      |
| 450 MHz                                                                       |         | –    | 15        | 17    | dB      |
| 870 MHz                                                                       |         | –    | 16        | –     | dB      |
| 1000 MHz                                                                      |         | –    | 17        | –     | dB      |
| Third Order Intercept Point (Input)                                           |         |      |           |       |         |
| 100 MHz                                                                       |         | –    | 18        | –     | dBm     |
| 450 MHz                                                                       |         | –    | 15        | –     | dBm     |
| 1000 MHz                                                                      | 26      | –    | 11        | –     | dBm     |
| Second Order Intercept Point (Input)                                          |         |      |           |       |         |
| 100 MHz to 600 MHz                                                            | 25      | –    | 79        | –     | dBm     |
| 600 MHz to 1000 MHz                                                           | 25a     | –    | 70        | –     | dBm     |
| 1dB Compression Point (Input)                                                 | 24, 24a | –    | 0         | –     | dBm     |
| Image Rejection (I/Q Gain/Phase Matching)                                     |         |      |           |       |         |
| LO Phase Correction On                                                        |         | 30   | 40        | –     | dB      |
| LO Phase Correction Off                                                       | 24      | 25   | –         | –     | dB      |
| I/Q Amplitude Balance                                                         |         |      |           |       |         |
| LO Phase Correction On                                                        |         | –    | ± 0.03    | ± 0.2 | dB      |
| LO Phase Correction Off                                                       | 24      | –    | ± 0.1     | –     | dB      |
| I/Q Phase Balance                                                             |         |      |           |       |         |
| LO Phase Correction On                                                        |         | –    | ± 0.5     | ± 2.0 | deg.    |
| LO Phase Correction Off                                                       | 24      | –    | ± 1       | ± 3   | deg.    |
| I/Q DC Offset Correction Steps                                                | 22      | 12   | 20        | 28    | mV      |
| I/Q DC Offset at Maximum Attenuation                                          | 20a     | –    | ±15       | ±55   | mV      |
| I/Q Output Bandwidth                                                          | 23      | –    | –         | 1.6   | MHz     |
| LO Divider Ratios (selectable)                                                |         | –    | 2, 4 or 6 | –     |         |
| LO Divider Noise Floor                                                        |         | –    | -152      | –     | dBc/Hz  |
| I/Q Differential Output Voltage Swing                                         | 20      | –    | –         | 4.0   | Vp-p    |
| Blocking                                                                      | 21      | 93   | 96        | –     | dB      |

Notes: 20. This is the maximum swing to guarantee meeting the third order distortion characteristics under the specified conditions and is not the maximum limiting value. For clarity, this means that the device has the capability to produce +/-1 V on each of the differential outputs. The outputs are capable of driving a load resistance across the differential outputs of 1 kΩ. This voltage output capability provides easy interfacing to other CML devices, like the CMX983 or CMX7164/7364, which has a maximum input signal amplitude of 2.4 Vp-p.

20a  $V_{\text{offset}}$  minimised using  $V_{\text{corr}}$  at minimum attenuation then with maximum baseband attenuation set  $V_{\text{offset}}$  is measured, mixer RF input terminated in 50 Ohms; see also section 8.1.2.

21. Test method based on EN 300 166; including operation of selectable dividers.

22. Register \$12, b2 = '0'.
23. This is the maximum bandwidth of the I and Q output signals with no external capacitors fitted and with the filter calibration circuit disabled. The bandwidth of the I/Q output can be adjusted to suit the application by use of the I/Q filters. This bandwidth can be set by using external capacitors (see sections 6.2.2 and 6.2.3). Note that a 25 kHz bandwidth on the I/Q filters supports a modulation signal bandwidth of 50 kHz.
24. Measured at 450 MHz.
- 24a Measured with baseband attenuations settings of 30 dB and above, with less attenuation measurement is limited by the output compression point.
25. Average value of IIP2 measurements at  $\pm 1$  MHz,  $\pm 5$  MHz and  $\pm 10$  MHz offsets using differential signals on I and Q channels, measurements every 100 MHz over the range 100 MHz to 600 MHz.
- 25a Average value of IIP2 measurements at  $\pm 1$  MHz,  $\pm 5$  MHz and  $\pm 10$  MHz offsets using differential signals on I and Q channels, measurements at 600 MHz and every 50 MHz over the range 700 MHz to 1000 MHz; phase correction off.
26. Phase correction off (\$15 b1='1' and b0='1'); Note: at 1 GHz better IIP3 performance can be obtained with phase correction off.

| Rx Direct Conversion Mixers                           | Notes  | Min. | Typ. | Max. | Units    |
|-------------------------------------------------------|--------|------|------|------|----------|
| Gain                                                  |        |      |      |      |          |
| 450 MHz                                               | 27     | –    | 17   | –    | dB(V/V)  |
| 940 MHz                                               |        | –    | 17   | –    | dB(V/V)  |
| Noise Figure                                          |        |      |      |      |          |
| 450 MHz                                               | 28     | –    | 13.5 | –    | dB       |
| Third Order Intercept Point (Input)                   |        |      |      |      |          |
| 450 MHz                                               | 28, 24 | –    | 11   | –    | dBm      |
| Input Frequency Range                                 | 15     | 100  | –    | 1000 | MHz      |
| LO Frequency Range before internal division           | 15     | 200  | –    | 2000 | MHz      |
| Input Impedance                                       | 30     | –    | –    | –    | $\Omega$ |
| Zero-IF Signal Bandwidth                              |        |      |      |      |          |
| at mixer output with CMX994EF baseband                |        | 1    | 1.6  |      | MHz      |
| LO Leakage at Operating Frequency (all divider modes) | 29     | -    | -90  | -    | dBm      |
| LO Frequency Leakage at Input div 2                   | 29     | –    | -65  | –    | dBm      |
| LO Frequency Leakage at Input div 4                   | 29     | –    | -75  | –    | dBm      |

- Notes:
- 27. Measured from matched input source.
  - 28. This is an indicative specification only as the parameter cannot be independently measured other than as part of the complete Rx Path.
  - 29. Measured with mixer input matched to 450 MHz.
  - 30. For further details see section 5.2.

| <b>Zero IF Amplifiers and Filters</b> | <b>Notes</b> | <b>Min.</b> | <b>Typ.</b> | <b>Max.</b> | <b>Units</b> |
|---------------------------------------|--------------|-------------|-------------|-------------|--------------|
| Gain                                  | 27, 31       | –           | 32          | –           | dB(V/V)      |
| Noise Figure                          | 28           | –           | –           | 10          | dB           |
| Third Order Intercept Point (Output)  | 28,31a       | –           | >50         | –           | dBm          |
| Output Impedance                      |              | –           | 20          | –           | $\Omega$     |
| 1dB Compression Point                 | 28           | -30         | –           | –           | dBm          |
| VGA Control Range                     | 32           | –           | 42          | –           | dB           |
| VGA Step Size                         |              | 4           | 6           | 8           | dB           |
| I/Q Output Bandwidth                  |              | –           | –           | 1.6         | MHz          |
| I/Q Differential Output Voltage Swing | 20           | –           | –           | 4.0         | Vp-p         |
| I/Q Output Common Mode                |              | –           | $AV_{DD}/2$ | –           | V            |
| <b>Post Mixer Filter</b>              |              |             |             |             |              |
| Bandwidth (-3dB)                      | 33, 38       | –           | 88          | –           | kHz          |
| <b>Adjacent Channel Rejection</b>     |              |             |             |             |              |
| Bandwidth (-3dB)                      | 33           | –           | 2           | –           | kHz          |
| Scaling Factors                       |              | –           | 1 : 2 : 4   | –           |              |
| Bandwidth Variation                   | 34           | –           | –           | 5           | %            |
| <b>Third Order Intermodulation</b>    |              |             |             |             |              |
| Post Mixer Filter                     | 28, 36       | –           | 90          | –           | dBc          |
| 1 <sup>st</sup> Amplifier             | 28, 36       | 85          | –           | –           | dBc          |
| 2 <sup>nd</sup> Amplifier             | 28, 37       | 85          | –           | –           | dBc          |

- Notes:
31. The first amplifier stage has nominal gain of 15 dB, the second stage has nominal gain of 22 dB.
  - 31a. In-band intermodulation calculated from output signal assuming 50 $\Omega$  impedance.
  32. Eight VGA steps.
  33. Assumes the recommended external capacitors are used (see section 5.2.2).
  34. Assuming external resistors with 1% tolerance and external capacitors with 5% tolerance.
  35. Tested at maximum gain setting of VGA.
  36. Assuming two 200 mVp-p tones at 25 kHz and 50 kHz.
  37. Assuming two 60 mVp-p tones at 25 kHz and 50 kHz.
  38. The post mixer filter bandwidth will vary with VGA setting. This may typically be 30%, with the bandwidth reducing at lower gain settings.

**AC Parameters – Tx Output**

| <b>Tx Divider</b>      | <b>Notes</b> | <b>Min.</b> | <b>Typ.</b>  | <b>Max.</b> | <b>Units</b> |
|------------------------|--------------|-------------|--------------|-------------|--------------|
| Input Frequency Range  |              | 100         | –            | 2000        | MHz          |
| Output Frequency Range |              | 100         | –            | 1000        | MHz          |
| Divider Ratio          |              | –           | 1, 2, 4 or 6 | –           |              |
| Output Level           | 39           | -5.5        | -3.5         | -1.5        | dBm          |
| Noise Floor            | 40           | –           | -146         | –           | dBc/Hz       |

- Notes: 39. 448 MHz output with LO divider ratio = 2; see section 8.3 for further information.  
 40. Noise at 5 MHz offset, measured at 500 MHz with 1 GHz Local Oscillator.

**AC Parameters – Integer N PLL / VCO and LO input**

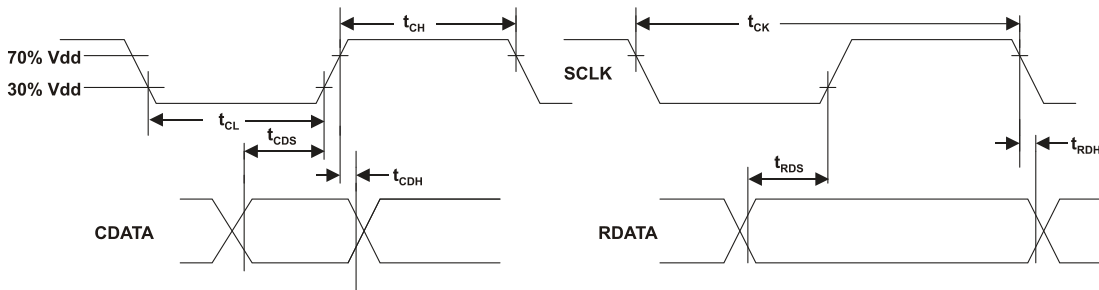
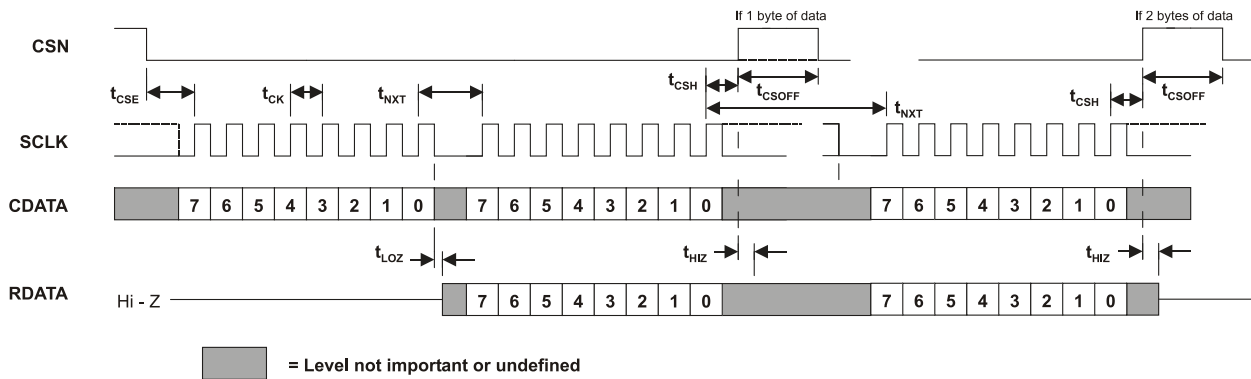
|                                                  | <b>Notes</b> | <b>Min.</b> | <b>Typ.</b> | <b>Max.</b> | <b>Unit</b> |
|--------------------------------------------------|--------------|-------------|-------------|-------------|-------------|
| <b>Phase Locked Loop</b>                         |              |             |             |             |             |
| <i>Reference Input</i>                           |              |             |             |             |             |
| Frequency                                        |              | 5           | –           | 30          | MHz         |
| Level                                            | 41           | 0.5         | –           | –           | Vp-p        |
| Divide Ratios (R Counter)                        |              | 2           | –           | 32767       |             |
| <i>Synthesiser</i>                               |              |             |             |             |             |
| Comparison Frequency ( $f_{\text{comparison}}$ ) |              | –           | –           | 500         | kHz         |
| Input Frequency Range                            |              | 200         | –           | 1100        | MHz         |
| Input Level                                      |              | -10         | -4          | –           | dBm         |
| Divide Ratios (M Counter)                        |              | 2           | –           | 262143      |             |
| Charge Pump Current                              |              | –           | $\pm 2.5$   | –           | mA          |
| 1Hz Normalised Phase Noise Floor                 | 44           | –           | -216        | –           | dBc/Hz      |
| <b>VCO Negative Resistance Amplifier</b>         |              |             |             |             |             |
| Frequency Range                                  | 43           | 200         | –           | 1100        | MHz         |
| Phase Noise at 10 kHz Offset                     | 42           | –           | -96         | –           | dBc/Hz      |
| Phase Noise at 100 kHz Offset                    | 42           | –           | -116        | –           | dBc/Hz      |
| <b>VCO Buffer</b>                                |              |             |             |             |             |
| Frequency Range                                  |              | 200         | –           | 1100        | MHz         |
| <b>LO Input</b>                                  |              |             |             |             |             |
| Input Level                                      | 45,46        | -15         | -10         | -5          | dBm         |
| Frequency Range                                  |              | 100         | –           | 2000        | MHz         |

- Notes: 41. Sinewave or clipped sinewave.  
 42. With external components forming a 750 MHz VCO and its LO divider value set to 4.  
 43. Operation will depend on the choice and layout of external resonant components.  
 44. 1 Hz Normalised Phase Noise Floor (PN1Hz) can be used to calculate the phase noise within the PLL loop bandwidth by: Measured Phase Noise (in 1Hz) =  $-PN1Hz - 20\log_{10}(M) - 10\log_{10}(f_{\text{comparison}})$   
 45. Single-ended input as described in section 5.3.1.  
 46. High levels of harmonic content in the LO signal should be avoided as I/Q balance can be degraded.

**AC Parameters – C-BUS**

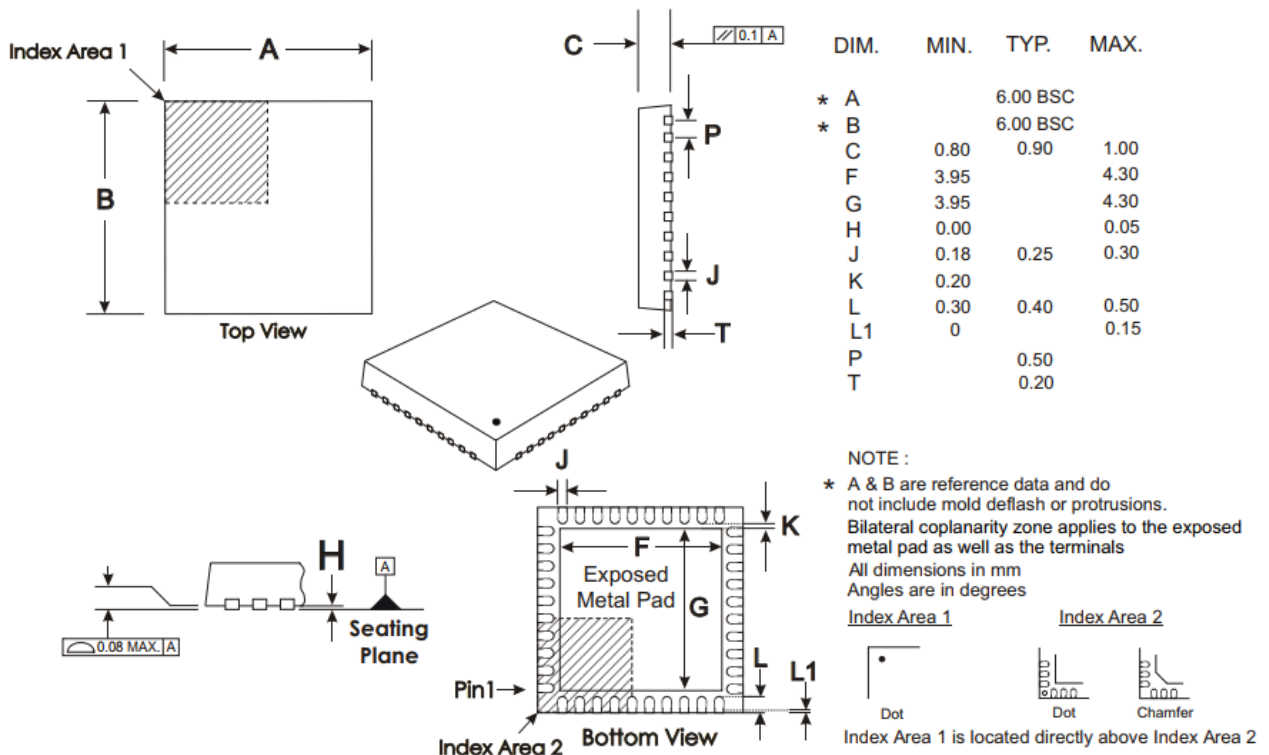
| C-BUS Timings (See Figure 30) | Notes                                 | Min. | Typ. | Max. | Units |
|-------------------------------|---------------------------------------|------|------|------|-------|
| t <sub>CSE</sub>              | CSN-enable to clock-high time         | 100  | –    | –    | ns    |
| t <sub>CSH</sub>              | Last clock-high to CSN-high time      | 100  | –    | –    | ns    |
| t <sub>LOZ</sub>              | Clock-low to reply output enable time | 0.0  | –    | –    | ns    |
| t <sub>HIZ</sub>              | CSN-high to reply output 3-state time | –    | –    | 1.0  | μs    |
| t <sub>CSOFF</sub>            | CSN-high time between transactions    | 1.0  | –    | –    | μs    |
| t <sub>NXT</sub>              | Inter-byte time                       | 200  | –    | –    | ns    |
| t <sub>CK</sub>               | Clock-cycle time                      | 200  | –    | –    | ns    |
| t <sub>CH</sub>               | Serial clock-high time                | 100  | –    | –    | ns    |
| t <sub>CL</sub>               | Serial clock-low time                 | 100  | –    | –    | ns    |
| t <sub>CDS</sub>              | Command data set-up time              | 75.0 | –    | –    | ns    |
| t <sub>CDH</sub>              | Command data hold time                | 25.0 | –    | –    | ns    |
| t <sub>RDS</sub>              | Reply data set-up time                | 50.0 | –    | –    | ns    |
| t <sub>RDH</sub>              | Reply data hold time                  | 0.0  | –    | –    | ns    |

Maximum 30 pF load on each C-BUS interface line.



**Figure 30 - C-BUS Timing**

## 9.2 Packaging



Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.

L minus L1 to be equal to, or greater than 0.3mm

The underside of the package has an exposed metal pad which should be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Notes:

1. In this device, the underside of the Q4 package should be electrically connected to the analogue ground. The circuit board should be designed so that no unwanted short circuits can occur.
2. As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: <https://cmlmicro.com/>.

Figure 31 - Q4 Mechanical Outline

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Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed

#### Contact information

For further information please contact your local CML sales representative.

Contact details can be found at [www.cmlmicro.com](http://www.cmlmicro.com)