CMX7158
Duplex Audio Scrambler

Duplex Frequency Inversion Scrambler

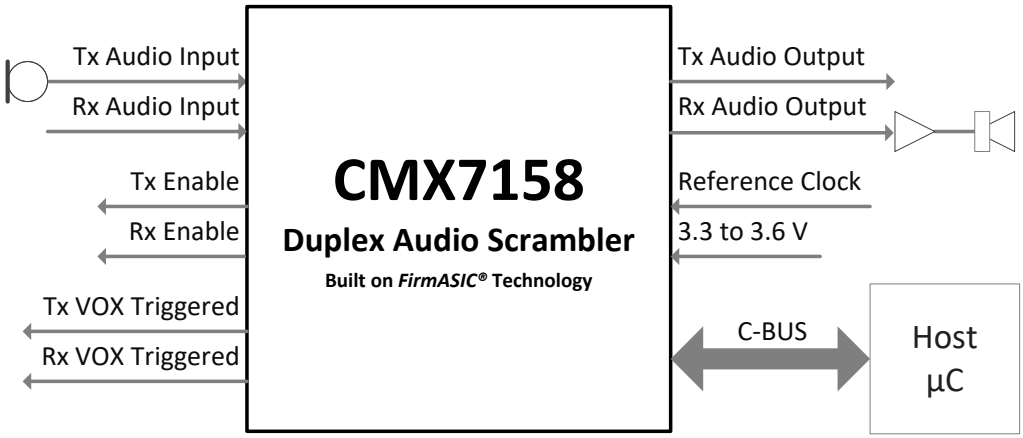
D/7158/2 October 2021 **DATASHEET** Provisional Information

Features

- **Fully independent Tx and Rx paths**
- **Programmable Inversion points**
- **MIC path AGC**
- **VOX detection**
- **DTMF encoder / decoder**
- **Selcall encoder / decoder**
- **Digital Gain Adjustment**
- **C-BUS Serial Interface to Host µController**
- **Bypass mode for HD Audio (up to 7kHz)**
- **Clear Mode**
- **TxENA and RxENA outputs**
- **Flexible Powersave Modes**
- **Low-power 3.0 to 3.6V Operation**
- **Small 48-pin Q3 VQFN Package**

Applications

- **Cellular radio accessories**
- **Bluetooth headsets**
- **PMR/LMR systems**
- **Wireless access control systems**
- **Intercom systems**
- **Wired telephony**



1 Brief Description

The CMX7158 is a full-duplex, frequency inversion audio scrambler IC. This makes it a suitable device for use in multi-function audio systems as well as mobile and hand portable Cellular / Bluetooth / PMR / LMR radio systems.
The device provides additional functionality to facilitate implementation including DTMF and Selcall signalling, VOX detection on both channels and a MIC AGC.

There are flexible power-saving modes and the device is available in a 48-pin VQFN Q3 package suitable for use with the PE0402 evaluation kit.

The device is derived from CML's proprietary *FirmASIC*® component technology. A function image™ that defines the device's functionality is loaded at power up.

CONTENTS

History

Version	Changes	Date
2	Section 3.1.4, Parametric Performance, AC Parameters, Audio Scrambler: corrected maximum inversion frequency Section 7.6.1, Audio Receive Mode, Audio De-scrambling: corrected default inversion frequency.	29th September 2021
1	First public release	17th June 2019
B	8.1.20: Clarified bit allocations in $C1 3, 7.7, 8.2: corrected TXENA operates with $C1:b7 not b1 11: added PE0402 overlay drawing	
A	Advanced Draft	1st February 2018

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document.

2 Block Diagram

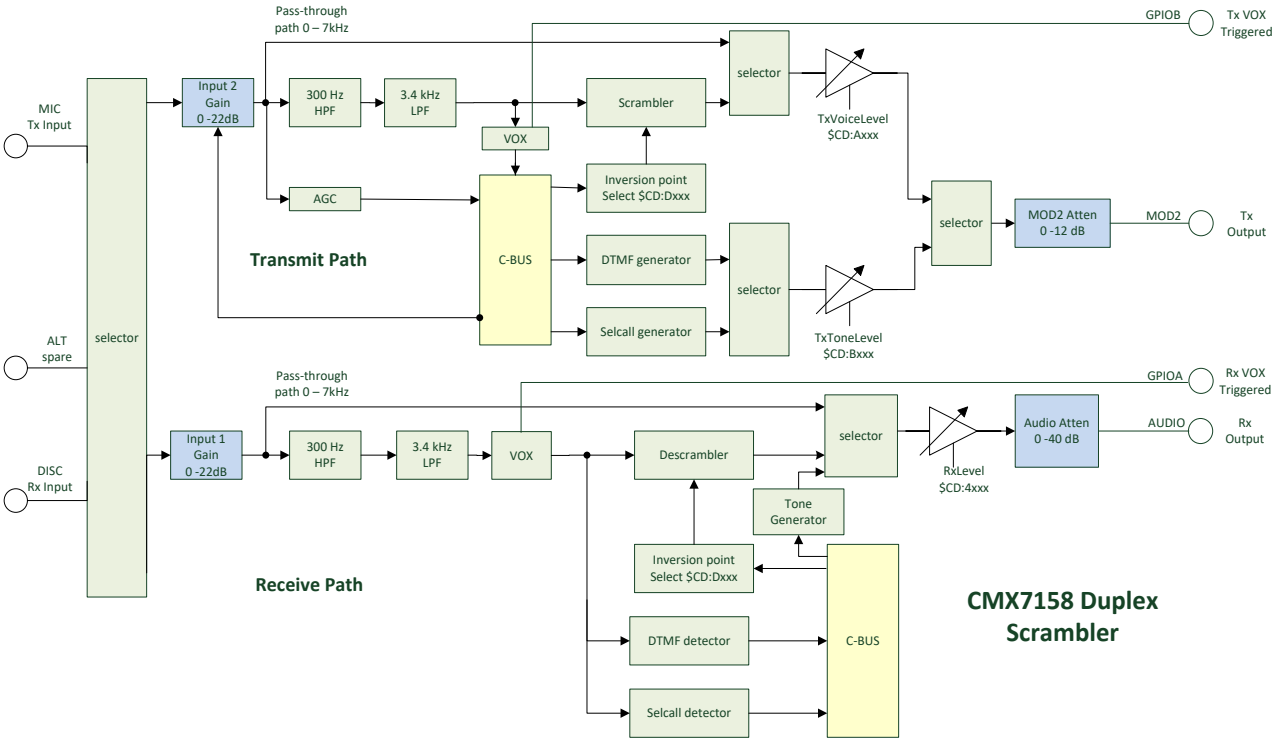


Figure 1 Block Diagram

3 Performance Specification

3.1 Electrical Performance

3.1.1 Absolute Maximum Ratings – typical figures

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	–0.3	4.5	V
AV_{DD}- AV_{SS}	–0.3	4.5	V
Voltage on any pin to DV_{SS}	–0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	–0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding V_{BIAS}) (i.e. V_{DEC}, AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS})	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

3.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
DVDD – DVSS		3.0	3.6	V
AVDD – AVSS		3.0	3.6	V
VDEC – DVSS	12	2.25	2.75	V
Operating Temperature		–40	+85	°C
XTAL/CLK Frequency (using a Xtal)	11	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	11	3.0	24.576	MHz

Notes: 11 Nominal XTAL/CLK frequency is 6.144MHz.
12 The V_{DEC} supply is automatically created from DV_{DD} by the on-chip voltage regulator.

3.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 3.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 6.144MHz ±0.01% (100ppm); Tamb = −40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage gain = 0dB.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	8	100	µA
AI_{DD} (AV_{DD} = 3.3V)		–	4	20	µA
IDLE Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	1.12	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	250	–	µA
Rx Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	6.80	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	3.05	–	mA
Tx Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	6.33	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	6.90	–	mA
XTAL/CLK	25				
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		−40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Leakage Current (Logic 1 or 0)	21	−1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic 1 (I_{OH} = 120µA	)	90%	–	–	DV_{DD}
(I_{OH} = 1mA)		80%			DV_{DD}
Output Logic 0 (IOL = 360µA)		–	–	10%	DV_{DD}
(I_{OL} = -1.5mA)		–	–	15%	DV_{DD}
"Off" State Leakage Current	21	–	–	10	µA
IRQN (V_{out} = DV_{DD})		-1.0		+1.0	µA
RDATA (output HiZ)		-1.0		+1.0	µA
V_{BIAS}	26				
Output Voltage Offset wrt AV_{DD}/2 (I_{OL} <1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes:
21 T_{amb} = 25°C. Not including any current drawn from the device pins by external circuitry.
22 Auxiliary circuits, audio Scrambler VOX disabled, but all other digital circuits (including the Main Clock PLL) enabled. A single analogue path is enabled through the device.
25 Characteristics when driving the XTAL/CLK pin with an external clock source.
26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 3.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' Pulse Width		31	15	–	–	ns
'Low' Pulse Width		31	15	–	–	ns
Input Impedance (measured at 6.144MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	400	–	ms
V_{BIAS}						
Start-up Time (from powersave)			–	30	–	ms
Microphone, Signal and Discriminator Inputs (MIC, ALT, DISC)						
Input Impedance		34	–	1	–	MΩ
Maximum Input Level (p-p)		35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)			80	–	–	kΩ
Amplifier Open Loop Voltage Gain (I/P = 1mV rms at 100Hz)			–	60	–	dB
Unity Gain Bandwidth			–	1.0	–	MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)		37	–0.5	0	+0.5	dB
Cumulative Gain Error (wrt gain at 0dB)		37	–1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

34 With no external components connected.

35 Centred about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, ALTFB OR MICFB

37 Design value for this block only in test mode. Overall gain input to output has a tolerance of 0dB ±1.0dB.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 2 and Audio Output (MOD2, AUDIO)						
Power-up to Output Stable		41	–	50	100	µs
Modulator Attenuators						
Attenuation (at 0dB)		43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)			−0.6	0	+0.6	dB
Output Impedance	Enabled	42	–	600	–	Ω
	Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)			–	–	±125	µA
Output Voltage Range		44	0.5	–	AV_{DD} –0.5	V
Load Resistance			20	–	–	kΩ
Audio Attenuator						
Attenuation (at 0dB)		43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)			−1.0	0	+1.0	dB
Output Impedance	Enabled	42	–	600	–	Ω
	Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)			–	–	±125	µA
Output Voltage Range		44	0.5	–	AV_{DD} –0.5	V
Load Resistance			20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

3.1.4 Parametric Performance

For the following conditions unless otherwise specified:
External components as recommended in Figure 3.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 6.144MHz ±0.003% (30ppm); Tamb = −40°C to +85°C.
AV_{DD} = DV_{DD} = CPV_{DD} = 3.0V to 3.6V; RFVDD = 2.25V to 2.75V.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.
All figures quoted in this section apply to the device when loaded with FI 1.0.x.x only. The use of other Function Images™, can modify the parametric performance of the device.

AC Parameters (cont.)		Notes	Min.	Typ.	Max.	Unit
Inband Tone Detector						
Sensitivity	(Pure Tone)		–	−26	–	dB
Response Time	(Good Signal)		–	35	–	ms
De-response Time	(Good Signal)		–	–	45	ms
Drop-out Immunity		76	–	–	20	ms
Frequency Range	(Inband Tone)		288	–	3000	Hz
Detection BW	(will decode)		-	+/-1.3	-	%
	(will not decode)		-	+/-2.7	-	%

Notes:
76 Immunity to signal drop-outs of up to the specified duration.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
DTMF Decoder					
Sensitivity		–	−22	+3	dB
Response Time		–	35	–	ms
De-response Time		–	–	45	ms
Falsing Rate (per 30min Voice input)		–	10	–	
Frequency Tolerance		–	±2.5	–	%
Twist		−10	–	+10	dB
Inband Tone Encoder					
Frequency Range		288	–	3000	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance	83	−1.0	0	+1.0	dB
Total Harmonic Distortion	82	–	2.0	4.0	%
DTMF Encoder					
Output Signal Level	84	–	775	–	mVrms
Output Level Variation					dB
Output Distortion		–	–	5	%
Rx Audio Tone Generator					
Output Signal Level	84	–	775	–	mVrms
Frequency Range		300		3400	Hz
Output Distortion		–	5	-	%

Notes:
82 Measured at MOD2 output.
83 AV_{DD} = 3.3V and Tx Audio Level set to 871mV p-p (308mVrms).
84 AV_{DD} = 3.3V.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Analogue Channel Audio Filtering					
Pass-band (nominal bandwidth):					
Audio	91	300	–	3400	Hz
Pass-band Gain (at 1.0kHz)		–	0	–	dB
Pass-band Ripple (wrt gain at 1.0kHz)		−2.0	0	+0.5	dB
Stop-band Attenuation		33.0	–	–	dB
Residual Hum and Noise Tx		–	−47	–	dBm
Residual Hum and Noise Rx		–	−74	–	dBm
Audio Scrambler					
Inversion Frequency	98	2632	3700	3900	Hz
Pass-band	99	300	–	3400	Hz

Notes: 91 The receiver audio filter complies with the characteristic shown in Figure 7.

98 Use of a scrambler inversion frequency other than 3700Hz will shift the scrambled voice signal outside the audio band, so that some of the signal will be lost in the channel filter. The result is that the descrambled voice signal will have a restricted bandwidth. The limits quoted are subjective and relate to the onset of a loss of speech intelligibility.

99 -6dB points, assuming default inversion frequency in use.

3.2 C-BUS Timing

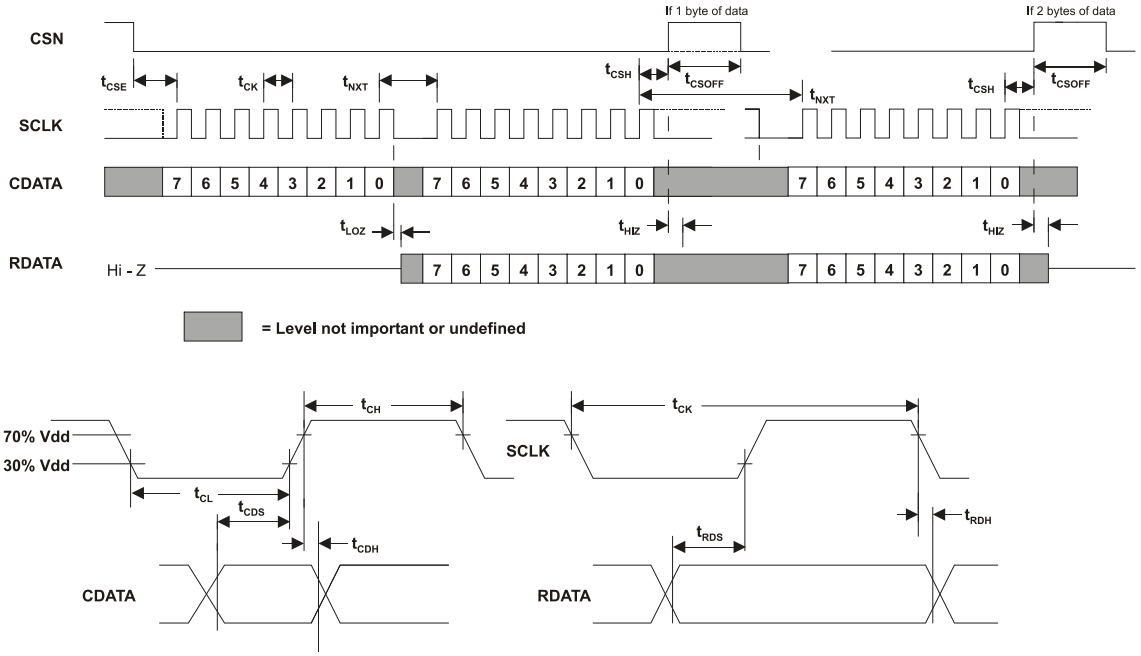


Figure 2 C-BUS Timing

C-BUS Timings		Min.	Typ.	Max.	Units
t_{CSE}	CSN-enable to clock-high time	100	–	–	ns
t_{CSH}	Last clock-high to CSN-high time	100	–	–	ns
t_{LOZ}	Clock-low to reply output enable time	0.0	–	–	ns
t_{HIZ}	CSN-high to reply output 3-state time	–	–	1.0	µs
t_{CSOFF}	CSN-high time between transactions	1.0	–	–	µs
t_{NXT}	Inter-byte time	200	–	–	ns
t_{CK}	Clock-cycle time	200	–	100	ns
t_{CH}	Serial clock-high time	100	–	–	ns
t_{CL}	Serial clock-low time	100	–	–	ns
t_{CDS}	Command data set-up time	75.0	–	–	ns
t_{CDH}	Command data hold time	25.0	–	–	ns
t_{RDS}	Reply data set-up time	50.0	–	–	ns
t_{RDH}	Reply data hold time	0.0	–	–	ns

Notes: 1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than earlier C-BUS timing specification. The CMX7158 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

4 Pin and Signal List

Q3-48pin	Name	Type	Description
1	-	NC	Reserved – do not connect this pin
2	-	NC	Reserved – do not connect this pin
3	-	NC	Reserved – do not connect this pin
4	-	NC	Reserved – do not connect this pin
5	BOOTEN1	IP	
6	BOOTEN2	IP	
7	DVSS	PWR	Digital Ground.
8	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
9	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for optional connection to RFV_{DD}.
10	RXENA	OP	Rx Enable – active low when in Rx mode ($C1:b0 = 1)
11	GPIOA	OP	Rx VOX triggered
12	GPIOB	OP	Tx VOX triggered
13	-	NC	Reserved – do not connect this pin
14	DVSS	PWR	Digital Ground.
15	TXENA	OP	Tx Enable – active low when in Tx mode ($C1:b7 = 1)
16	DISCN	IP	DISC inverting input.
17	DISCFB	OP	DISC amplifier feedback.
18	ALTN	IP	ALT inverting input.
19	ALTFB	OP	ALT amplifier feedback.
20	MICFB	OP	MIC amplifier feedback.
21	MICN	IP	MIC inverting input.
22	AVSS	PWR	Analogue Ground.
23	-	NC	Reserved – do not connect this pin
24	MOD2	OP	TX output.
25	VBIAS	OP	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when VBIAS will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed.
26	AUDIO	OP	RX output.
27		NC	Reserved – do not connect this pin
28		NC	Reserved – do not connect this pin
29		NC	Reserved – do not connect this pin
30		NC	Reserved – do not connect this pin
31	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuits. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.

Q3-48pin	Name	Type	Description
32	-	OP	Reserved – do not connect this pin
33	-	OP	Reserved – do not connect this pin
34	AVSS	PWR	Analogue Ground.
35	-	OP	Reserved – do not connect this pin
36	-	OP	Reserved – do not connect this pin
37	DVSS	PWR	Digital Ground.
38	VDEC	PWR	Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for the optional connection to RFV_{DD}.
39	XTAL/CLK	IP	Input to the oscillator inverter from the Xtal circuit or external clock source.
40	XTALN	OP	The output of the on-chip Xtal oscillator inverter.
41	DVDD	PWR	The 3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVss by capacitors mounted close to the device pins.
42	CDATA	IP	C-BUS: Serial data input from the µC.
43	RDATA	TS OP	C-BUS: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
44	-	NC	Reserved – do not connect this pin.
45	DVSS	PWR	Digital Ground.
46	SCLK	IP	C-BUS: The C-BUS serial clock input from the µC.
47	-	OP	Reserved – do not connect this pin
48	CSN	IP	C-BUS: The C-BUS chip select input from the µC - there is no internal pullup on this input.
EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on Q1 & Q3 packages only) may be electrically unconnected or, alternatively, may be connected to Analogue Ground (AVss). **No other electrical connection is permitted.**

IP = Input (+ PU/PD = internal pullup / pulldown resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal.

4.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltage

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
V_{DEC}	VDEC	Power supply for core logic, derived from DVDD by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AVDD
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits

5 Component and PCB Recommendations

5.1 Recommended External Components

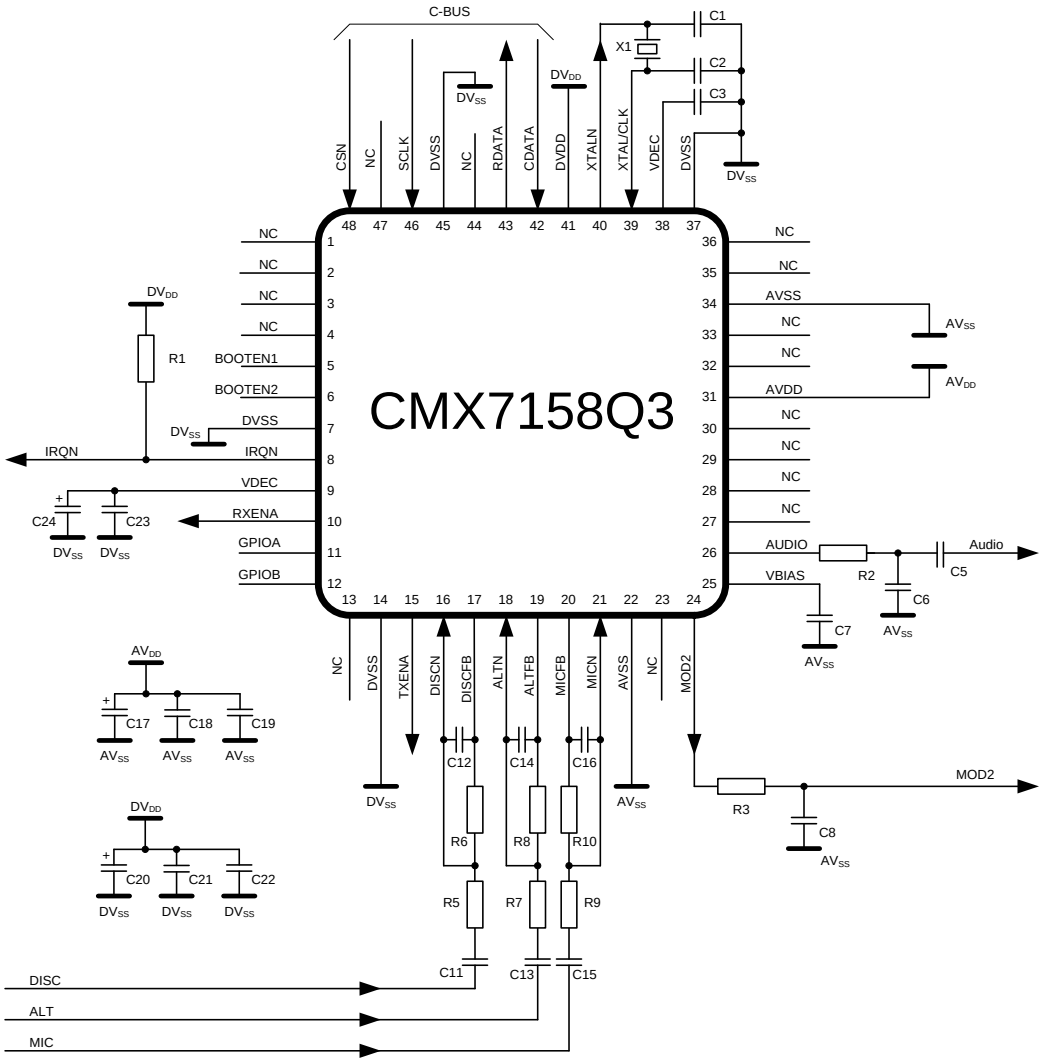


Figure 3 CMX7158 Recommended External Components

Table 2 Recommended External Components (typical example)

R1	100kΩ	C1	18pF	C11	See note 5	C21	10nF
R2	100kΩ	C2	18pF	C12	100pF	C22	10nF
R3	100kΩ	C3	10nF	C13	See note 5	C23	10nF
R4		C4	*not used*	C14	180pF	C24	10µF
R5	See note 2	C5	1nF	C15	See note 5		
R6	100kΩ	C6	100pF	C16	180pF		
R7	See note 3	C7	100nF	C17	10µF		
R8	100kΩ	C8	100pF	C18	10nF	X1	6.144MHz
R9	See note 4	C9		C19	10nF		See note 1
R10	100kΩ	C10	*not used*	C20	10µF		

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, a 6.144MHz clock is selected, other values could be used if the various internal clock dividers are set to appropriate values.

2. R5 should be selected to provide the desired dc gain (assuming C11 is not present) of the DISC input, as follows:

$$|GAIN_{DISC}| = 100k\Omega / R5$$

   The gain should be such that the resultant output at the DISCFB pin is within the input signal range specified in 7.10.

3. R7 should be selected to provide the desired dc gain (assuming C13 is not present) of the ALT input as follows:

$$|GAIN_{ALT}| = 100k\Omega / R7$$

   The gain should be such that the resultant output at the ALTFB pin is within the input signal range specified in 7.10.

4. R9 should be selected to provide the desired dc gain (assuming C15 is not present) of the MIC input as follows:

$$|GAIN_{MIC}| = 100k\Omega / R9$$

   The gain should be such that the resultant output at the MICFB pin is within the input signal range specified in 7.10. For optimum performance with low signal microphones, an additional external gain stage may be required.

5. C11, C13 and C15 should be selected to maintain the lower frequency roll-off of the MIC, ALT and DISC inputs as follows:

$$C11 \geq 1.0\mu F \times |GAIN_{DISC}|$$

$$C13 \geq 1.0\mu F \times |GAIN_{ALT}|$$

$$C15 \geq 1.0\mu F \times |GAIN_{MIC}|$$

6. ALT and ALTFB connections allow the user to have an additional signal input (usually assigned to the External Signalling). Component connections and values are as for the respective DISC and MIC networks. If this input is not required, the ALT pin should be connected to AVss.

7. C5 (AUDIO output) should be increased to 1.0µF if frequencies below 300Hz need to be used on this pin.

8. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both VDEC pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each VDEC pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both VDEC pins.

5.2 PCB Layout Guidelines and Power Supply Decoupling

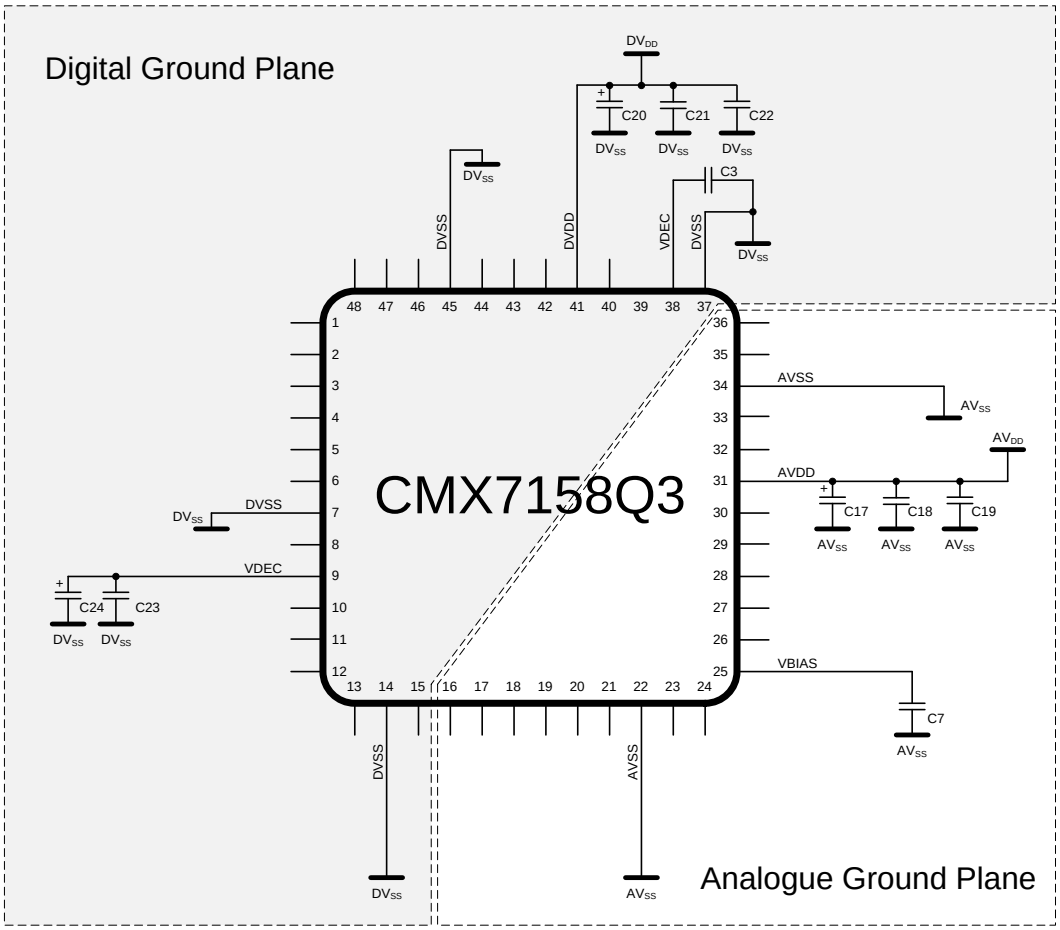


Figure 4 CMX7158 Power Supply and Decoupling

Component Values as per Table 2

Notes:

It is important to protect the analogue pins from extraneous in-band noise and to minimise the impedance between the device and the supply and bias decoupling capacitors. The decoupling capacitors C3, C7, C18, C19, C21, C22 and C24 should be as close as possible to the device. It is therefore recommended that the printed circuit board be laid out with separate ground planes for the AV_{SS} and DV_{SS} supplies in the area of the CMX7158, with provision to make links between them, close to the device. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it must be buffered with a high input impedance buffer.

The single ended microphone input and audio output must be ac coupled (as shown), so that their return paths can be connected to AV_{SS} without introducing dc offsets. Further buffering of the audio output is advised.

The crystal X1 may be replaced with an external clock source.

.

6 General Description

The CMX7158 is a full-duplex, audio band frequency-inversion scrambler IC, suitable for use in multi-function mobile and hand-portable PMR/LMR radio systems.

Encoder and decoder functions are also provided for Selcall and DTMF signalling.

The CMX7158 includes a crystal clock generator with buffered output, to provide a common system clock if required. A block diagram of the CMX7158 is shown in Figure 1.

The signal processing blocks can be individually assigned to any one of three signal inputs.

Tx Functions:

- Single/dual microphone with input amplifier and programmable gain
- Selectable frequency inversion voice scrambling
- 300Hz HPF and 3.4kHz LPF
- Output with programmable level adjustment
- MIC AGC
- Bypass / Clear / Scrambled mode
- Programmable VOX detector and output
- Programmable Selcall generator
- Programmable DTMF generator
- Tx Enable output

Rx Functions:

- Single/dual inputs with input amplifier and programmable gain
- Selectable frequency inversion voice de-scrambling
- 300Hz HPF and 3.4kHz LPF
- Software volume control
- Bypass / Clear / Scrambled mode
- Programmable VOX detector and output
- Selcall decoder
- DTMF decoder
- Programmable audio tone generator
- Rx Enable output

Interface:

- C-BUS, 4-wire high-speed synchronous serial command/data bus
- Open drain IRQ to host

7 Detailed Descriptions

7.1 Xtal Frequency

The CMX7158 is designed to work with a Xtal of 6.144MHz. If this default configuration is not used, then Program Block 3 (see section 10.2.4) should be loaded with the correct values to ensure that the device will work to specification with the user specified clock frequency. A table of common values can be found in Table 3. Note the maximum Xtal frequency is 12.288MHz, although an external clock source of up to 24.576MHz can be used.

The register values in Table 3 are shown in hex (however not all bits are relevant, see Program Block 3 for details), the default settings are shown in bold, and the settings which do not give an exact setting (but are within acceptable limits) are in italics. The new settings in P3.4-7 are implemented on a change to Rx or Tx mode.

Table 3 Xtal/clock Frequency Settings for Program Block 3

Program Block entry			External Frequency Source (MHz)							
			3.6864	**6.144**	9.216	12.0	12.8	16.368	16.8	19.2
P3.4	Rx or Tx	Ref clk divide	$018	**$020**	$030	$03E	$064	$0AA	$0AF	$064
P3.5		PLL clk divide	$280	**$200**	$200	$200	$300	$400	$400	$200
P3.6		VCO output and AUX clk divide	$13C	**$140**	$140	$140	$140	$140	$140	$140
P3.7		Internal ADC/DAC clk divide	$008	**$008**	$008	$008	$008	$008	$008	$008

7.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7158 and the host µC; this interface is compatible with microwire and SPI. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the Status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 10.1.3.

The CMX7158 will monitor the state of the C-BUS registers that the host has written to every 250µs (the C-BUS latency period) hence it is not advisable for the host to make successive writes to the same C-BUS register within this period.

To minimise activity on the C-BUS interface, optimise response times and ensure reliable data transfers, it is advised that the IRQ facility be utilised (using the IRQ mask register, $CE). It is permissible for the host to poll the IRQ pin if the host µC does not support a fully interrupt-driven architecture. This removes the need to continually poll the C-BUS status register ($C6) for status changes.

7.2.1 C-BUS Operation

The C-BUS block provides for the transfer of data and control or status information between the CMX7158's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single Address byte sent from the µC which may be followed by one or more Data byte(s) sent from the µC to be written into one of the CMX7158's Write Only Registers, or one or more data byte(s) read out from one of the CMX7158's Read Only Registers, as illustrated in Figure 5.

Data sent from the µC on the CDATA line is clocked into the CMX7158 on the rising edge of the SCLK input. RDATA sent from the CMX7158 to the µC is valid when SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an Address byte is dependent on the value of the Address byte. The most significant bit of the address or data are sent first. For detailed timings see section 7.3.. Note that, due to internal timing constraints, there may be a delay of up to 250µs between the end of a C-BUS write operation and the device reading the data from its internal register. Ensure that this C-BUS latency time (up to 250µs) is observed when writing multiple commands to the same C-BUS register.

7.3 C-BUS Timing

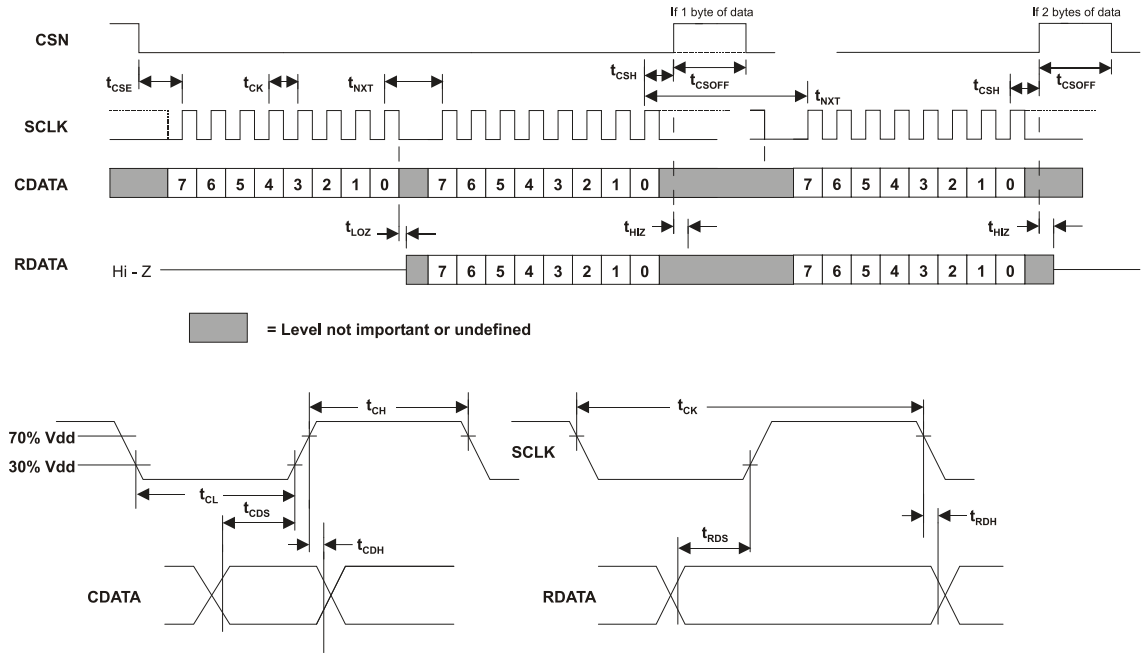


Figure 5 C-BUS Transactions

C-BUS Timings		Min.	Typ.	Max.	Units
t_{CSE}	CSN-enable to clock-high time	100	–	–	ns
t_{CSH}	Last clock-high to CSN-high time	100	–	–	ns
t_{LOZ}	Clock-low to reply output enable time	0.0	–	–	ns
t_{HIZ}	CSN-high to reply output 3-state time	–	–	1.0	µs
t_{CSOFF}	CSN-high time between transactions	1.0	–	–	µs
t_{NXT}	Inter-byte time	200	–	–	ns
t_{CK}	Clock-cycle time	200	–	100	ns
t_{CH}	Serial clock-high time	100	–	–	ns
t_{CL}	Serial clock-low time	100	–	–	ns
t_{CDS}	Command data set-up time	75.0	–	–	ns
t_{CDH}	Command data hold time	25.0	–	–	ns
t_{RDS}	Reply data set-up time	50.0	–	–	ns
t_{RDH}	Reply data hold time	0.0	–	–	ns

Notes: 1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than earlier C-BUS timing specification. The CMX7158 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

7.4 Device Initialisation

Device functionality is provided as a *FirmASIC*® Function Image file (7158FI1.x.x.x) for use with the CMX7040 / PE0402 / PE0003 for evaluation and test or the CMX7158 for production.

The Function Image™(FI) file, which defines the operational capabilities of the device, may be obtained from the CMLTechnical Portal, following product registration. This is in the form of a 'C' header file which can be downloaded using the PE0003 or included into the host controller software. The maximum possible size of Function Image™ is 46 kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are only read at power-on or following a C-BUS General Reset and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN pins are ignored until the next power-up or C-BUS General Reset.

7.4.1 Host Loading The Function Image

The BOOTEN pins are both fitted with internal low-current pulldown devices.

For C-BUS load operation, both pins should be pulled high by connecting them to V_{DD} either directly or via a 220kΩ resistor.

Once the FI has been loaded, the device performs these actions:

(1) the product identification code $7158 is reported in C-BUS register $C5
(2) the FI version code is reported in C-BUS register $C9
(3) the two 32-bit FI checksums are reported in C-BUS register pairs $A9, $AA and $B8, $B9
(4) the device initialises fully, enters idle mode and becomes ready for use, and the Programming Flag (bit 0 of the Status register, $C6) will be set.

The checksums should be verified against the published values to ensure that the FI has loaded correctly. Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and become unresponsive to all further host commands (including General Reset). A power-on reset is required to recover from this state.

The checksum values are available from the CML Technical Portal.

Table 4 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS Host load	1	1
reserved	1	0
reserved	0	1
No FI load	0	0

Note: In the rare event that a General Reset needs to be issued without the requirement to re-load the FI, the BOOTEN pins must both be cleared to '0' before issuing the Reset command. The Checksum values will be reported. There will not be any FI loading delay. This assumes that a valid FI has been previously loaded and that V_{DD} has been maintained throughout the reset to preserve the data.

Each time the device is powered up its Function Image™ must first be loaded. This assigns internal device resources and determines all device features. The device does not operate until the Function Image™ is loaded.

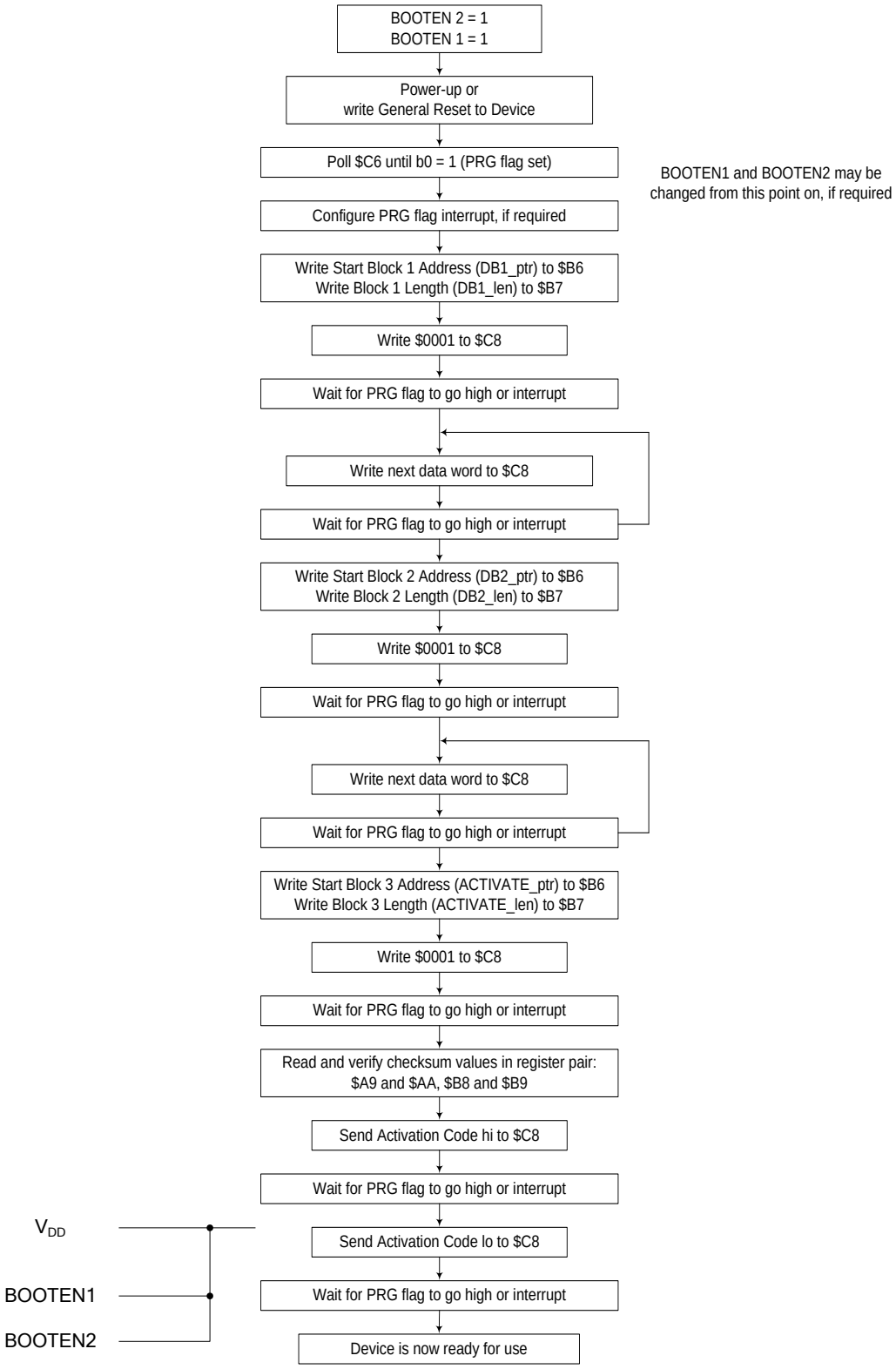


Figure 6 FI Loading From Host

The download time is limited by the clock frequency of the C-BUS, with a 5MHz SCLK, it should take less than 500ms to complete.

7.5 Device Control

The CMX7158 is controlled by reading and writing C-BUS registers.

To conserve power when the device is not actively processing an analogue signal, it should be placed in IDLE mode using the Mode Control ($C1) register. Additional powersaving can be achieved by disabling all unused hardware blocks using their control registers.

For basic active operation:

1. Set operating parameters using the Programming register ($C8)
2. Enable the required hardware sections using the Power Down Control ($C0) register
3. Select the required analogue Signal Routing and Gain ($B0 and $B1)
4. Use the Mode Control ($C1) register to place the device into Rx and/or Tx mode[1].

See:
- Powerdown Control - $C0 write
- Mode Control – $C1 write

7.5.1 Signal Routing

The CMX7158 offers a flexible analogue routing architecture with three signal inputs, two outputs and independent Rx and Tx signal processing paths. The Rx processing path is internally routed from Input1 to Output1, and the Tx path from Input2 to Output2. Input1 or Input2 can be routed from any of the three input signal amplifiers (DISC, ALT or MIC).

See:
- Input Gain and Output Signal Routing - $B1 write
- Mode Control – $C1 write

The analogue gain/attenuation of each input and output can be set individually, with additional fine gain control via the Programming register.

See:
- Analogue Output Gain - $B0 write
- Input Gain and Output Signal Routing - $B1 write

[1] To mitigate against signal transients during the power-on of the signal processing functions, it may be advisable to select the analogue signal routing AFTER the device has been placed in Rx or Tx mode.

7.5.2 Mode Control

The CMX7158 operates in two modes:

- IDLE mode
- Active mode (Rx and/or Tx operation)

At power-on or following a Reset or General Reset the device automatically enters IDLE mode. This state gives maximum power saving with all unused hardware blocks powered down, and also allows access to the Programming register for device configuration.

The host can then enable Rx and Tx signal processing functions as required for either half-duplex or full-duplex operation. When Rx and Tx are both disabled the device returns back to IDLE mode.

See:
- Mode Control – $C1 write

7.6 Audio Functions

7.6.1 Audio Receive Mode

The CMX7158 operates in full-duplex, so whilst in receive mode the transmit path (MIC input and MOD2 amplifiers) can be disabled and powered down if required. The AUDIO output signal level is equalised (to V_{BIAS}) before switching between the audio port and the modulator ports, to minimise unwanted audible transients. The Off/Powersave level at MOD2 output is the same as the VBIAS pin, so the audio output level must also be at this level before switching.

See:
- $C2 write

Receiving Audio Band Signals

When a voice-based signal is being received, it is up to the host µC, in response to signal status information provided by the CMX7158, to control muting/enabling of the audio signal to the AUDIO output.
The path through the device has a programmable gain stage. Whilst in receive mode this should normally be set to 0dB (the default) gain.

Receive Filtering

The incoming signal is filtered, as shown in Figure 7 (with the 300Hz HPF also active), to remove sub-audio components and to minimise high frequency noise. When appropriate, the audio signal can then be routed to the AUDIO output. Separate filters are available for:

- 300Hz High Pass (to reject sub-audible signalling)
- 3.4kHz Low Pass

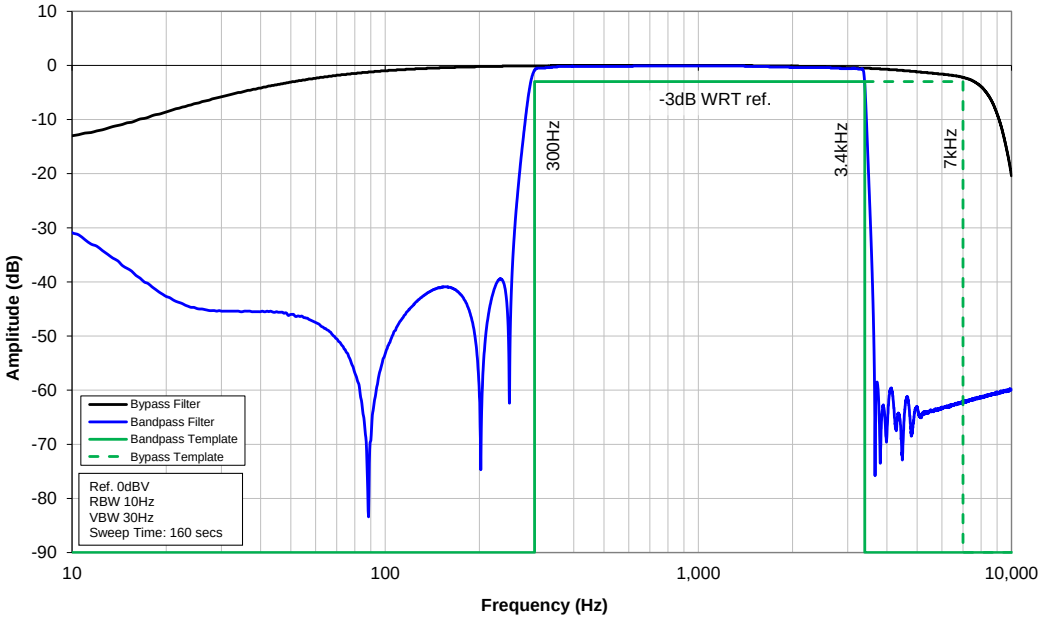


Figure 7 Audio Filter Frequency Response - Bypass and Bandpass Filters

Audio De-scrambling

The CMX7158 incorporates an optional frequency inversion de-scrambler in receive mode. This de-scrambles received audio band signals that have been scrambled in the transmitter. The inversion frequency defaults to 3700Hz, but may be modified by writing to $CD:Dxxx.
See:

- Audio Control - $CD write

7.6.2 Audio Transmit Mode

When the modulator outputs are disabled, their outputs will be set to V_{BIAS}. When the modulator output drivers are powered down, their outputs will be floating (high impedance). A programmable gain stage in the microphone input path facilitates a host controlled VOGAD capability, or an internal AGC function may be used.
See:

- Audio Control - $CD write
- Input Gain and Output Signal Routing - $B1 write

Processing Audio Signals for Transmission over Analogue Channels

The microphone input, with programmable gain, can be selected as the audio input source. . When the 300Hz HPF is enabled, it will attenuate sub-audio frequencies below 250Hz by more than 33 dB with respect to the signal level at 1kHz.

Tx Input AGC

An Automatic Gain Control system can be enabled by setting the relevant bits of the Program Block P4.11. The setting of the Input2 Gain stage is recorded when the device enters Tx mode and if the signal exceeds the pre-set threshold, the Input2 Gain is automatically reduced in 3.2dB steps until it falls within the operational levels or the range of the gain stage is exhausted. When the signal level drops, the gain will be automatically increased in 3.2dB steps at the rate set in P4.11 until the initial values has been reached. For maximum effect the system should be designed such that the +22.4dB setting of the Input2 Gain stage achieves the nominal levels. To ensure consistent operation, it is recommended that the Input2 Gain stage value be re-initialised before entering Tx mode.

- Input Gain and Output Signal Routing - $B1 write
- Program Block 4 – Gain and Offset Setup

Audio Scrambling

The Rx and Tx voice filter paths both include an optional frequency inversion. The inversion point defaults to 3700Hz which may be modified by writing to $CD:Dxxx.
See:

- Audio Control - $CD write

7.7 Selcall and DTMF

The CMX7158 supports DTMF, Selcall, and programmable Inband tones between 288Hz and 3000Hz. By default the CMX7158 loads the CCIR Selcall tone set but this may be overwritten by the host with any set of tones within its operational range using the Programming register. Some other standard tone sets are shown in Table 5. Note that the CMX7158 does not support automatic repeat tone insertion or deletion so it is up to the host to correctly implement the appropriate protocol. In Rx mode the DTMF and Selcall detectors can be enabled in parallel if required although this is not recommended due to the increased likelihood of false detects.

See:

- Mode Control – $C1 write
- Tx Inband Tones - $C3 write
- Tone Status - $CC read

7.7.1 Transmitting Selcall and DTMF Tones

Selcall and DTMF tones must be transmitted without any other signals in the audio band. To ensure this, the Tx voice path is automatically disabled when either tone generator is operating.

The Selcall or DTMF tone to be generated is specified in the Tx Inband Tones register ($C3), b14-11 for Selcall, b3-0 for DTMF. The tone output level can be adjusted using the Audio Control register, $CD:Bxxx.

Table 5 shows the Selcall tone set and numbering. The standard DTMF tone frequencies are shown in Table 6. Single tones and twist (lower frequency tone reduced by 2dB) can be enabled by setting the appropriate bits in the Tx Inband Tones register ($C3).

7.7.2 Receiving and Decoding Selcall Tones

Selcall and other Inband tones are typically used to flag the start of a call or confirm the end. If they occur during a call while the Rx voice path is enabled, the tone may be audible at the receiver output. It is up to the host to enable and disable the Rx voice path as appropriate.

The decoder will issue an interrupt (b13 of the Status register, $C6) whenever a valid Inband tone changes state (switches on, switches off or changes to different tone). The host should then read the Tone Status register ($CC) for further information. When a candidate tone is received the decoder scans through the tone table sequentially and the tone number reported will be the first one that matches the incoming frequency. When a valid tone switches off the Tone Status register is cleared. When a Selcall Tone is detected, b15 of $C3 will be set, the actual tone value will be available in b14-11.

Table 5 Inband Tones

Selcall Tones		
b14 - 11		Freq.
Dec	Hex	(Hz)
0	0	1981 (P1.2)
1	1	1124 (P1.3)
2	2	1197 (P1.4)
3	3	1275 (P1.5)
4	4	1358 (P1.6)
5	5	1446 (P1.7)
6	6	1540 (P1.8)
7	7	1640 (P1.9)
8	8	1747 (P1.10)
9	9	1860 (P1.11)
10	A	2400 (P1.12)
11	B	930 (P1.13)
12	C	2247 (P1.14)
13	D	991 (P1.15)
14	E	2110[1] (P1.16)
15	F	1055 (P1.17)

NOTE: Normally, tone 14 is the repeat tone. This code must be used in transmit mode when the new code to be sent is the same as the previous one: e.g. to send '333' the sequence '3R3' should be sent, where 'R' is the repeat tone. When receiving Selcall tones, the CMX7158 will indicate the repeat tone when it is received. It is up to the host to interpret and decode the tones accordingly.

7.7.3 Receiving DTMF Tones

DTMF tones are typically used to send addressing information at the start of a call. It is up to the host to enable and disable the Rx voice path as appropriate.

The decoder will issue an interrupt (b12 of the Status register, $C6) whenever a valid DTMF tone switches on or off. The host should then read the Tone Status register ($CC) for further information, b10 will be set to indicate a DTMF tone is available, the tone value will be available in b14-11.. The tone numbers are shown below in Table 6. When a valid tone switches off the Tone Status register is cleared.

Table 6 DTMF Tone Pairs

Tone Code (Hex)	Key Pad Position	Low Tone (Hz)	High Tone (Hz)
1	1	697	1209
2	2	697	1336
3	3	697	1477
4	4	770	1209
5	5	770	1336
6	6	770	1477
7	7	852	1209
8	8	852	1336
9	9	852	1477
A	0	941	1336
B	*	941	1209
C	#	941	1477
D	A	697	1633
E	B	770	1633
F	C	852	1633
0	D	941	1633

Note: When the 'Single Tone' bit is enabled, only the underlined tone is generated.

7.7.4 Alternative Selcall Tone Sets

These may be loaded via the Programming register to locations P1.2 to P1.17. See section 10.2.2..

Table 7 Alternative Selcall Tone Sets

Tone Number	Frequency (Hz)				
	EIA	EEA	CCIR	ZVEI 1	ZVEI 2
(P1.2) 0	600	1981	1981	2400	2400
(P1.3) 1	741	1124	1124	1060	1060
(P1.4) 2	882	1197	1197	1160	1160
(P1.5) 3	1023	1275	1275	1270	1270
(P1.6) 4	1164	1358	1358	1400	1400
(P1.7) 5	1305	1446	1446	1530	1530
(P1.8) 6	1446	1540	1540	1670	1670
(P1.9) 7	1587	1640	1640	1830	1830
(P1.10) 8	1728	1747	1747	2000	2000
(P1.11) 9	1869	1860	1860	2200	2200
(P1.12) A (10)	2151	1055	2400	2800	885
(P1.13) B (11)	2435	930	930	810	810
(P1.14) C (12)	2010	2247	2247	970	740
(P1.15) D (13)	2295	991	991	885	680
(P1.16) E (14)	459	2110	2110	2600	970
(P1.17) F (15)	NoTone	2400	1055	680	2600

7.8 Digital System Clock Generator

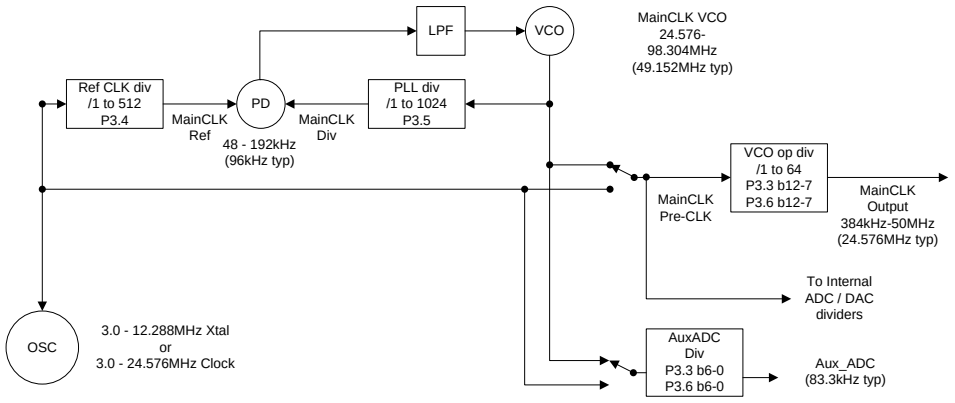


Figure 8 Digital Clock Generation Schemes

The CMX7158 includes a 2-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in section 5.1, or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but by default, a 6.144MHz Xtal is assumed for the functionality provided in the CMX7158.

7.8.1 Main Clock Operation

A PLL is used to create the main clock (MainCLK - nominally 24.576MHz) for the internal sections of the CMX7158. At the same time, other internal clocks are generated by division of either the Xtal Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters.

The CMX7158 defaults to the settings appropriate for a 6.144MHz Xtal, however if other frequencies are to be used then the Program Block P3.4 to P3.7 will need to be programmed appropriately at power-on. A table of common values is provided in Table 3..

See:

- Program Block 3 – Clock Control

7.9 GPIO

Two pins are provided for control of external hardware. RXENA and TXENA are driven by the device to follow the state of the Rx and Tx Mode bits in the Mode register, $C1:

$C1 Mode:	b7	b0	TXENA	RXENA
IDLE	0	0	1	1
Rx	0	1	1	0
Tx	1	0	0	1
Rx and Tx	1	1	1	1

7.10 Signal Level Optimisation

The internal signal processing of the CMX7158 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) – (2 x 0.3V)] Volts p-p = 838mVrms, assuming a sine wave signal. Compared to the reference level of 308mVrms, this is a signal of +8.69dB. This level should not be exceeded at any stage.

8 Evaluation

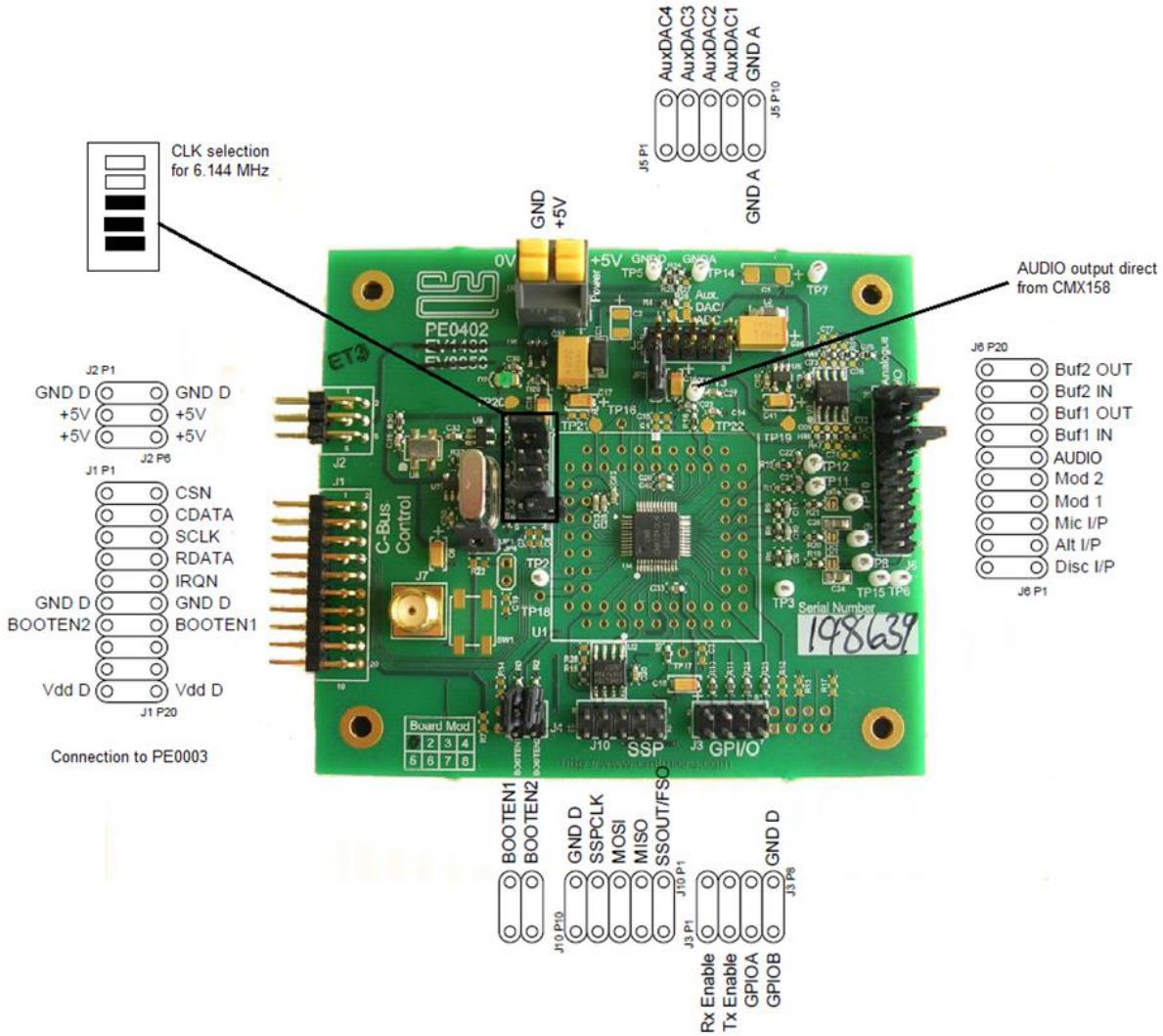
When using the PE0402 connected to a PE0003, the CML standard GUI can be used to load the Function Image and exercise the device. The C-BUS speed should be set to 5MHz in the options tab. The suggested signal routing is:

MIC -> Input 2 Output2 -> MOD2
DISC -> Input1 Output1 -> Audio

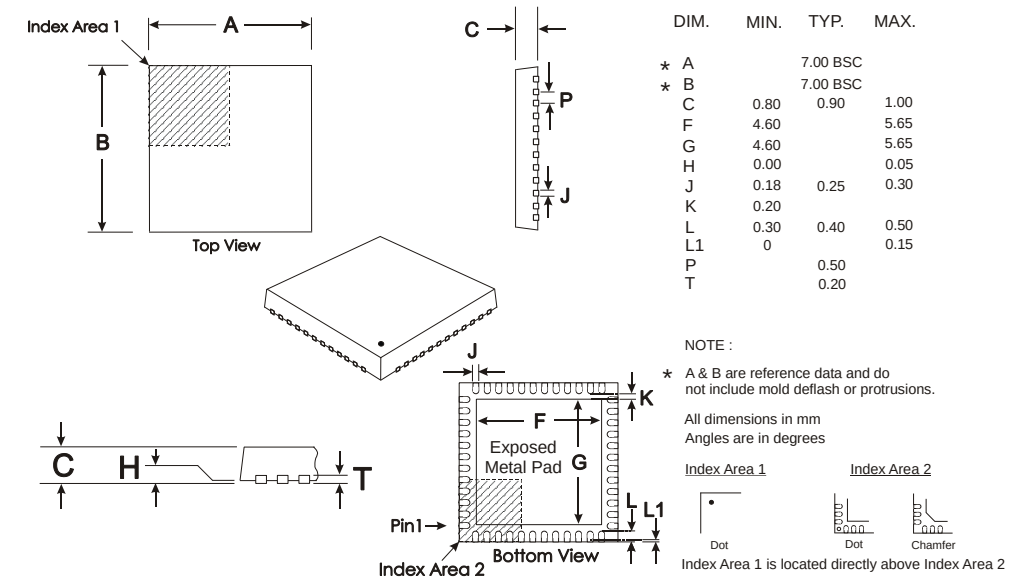
The following sequence will set the device up appropriately:

$C0 = $FFC4 Enable all hardware sections (this can be optimised to save power)
Readback $C4 to confirm communication, should read $FFC4
$B0 = $770F Output Gain settings
$C1 = $0303 Enable Tx and Rx paths in clear mode
$B1 = $00DC Signal Routing and Input Gain settings

Care should be taken to ensure that the components installed on the PE0402 do not filter the input and output signals unintentionally. In particular, C27 on the AUDIO output may need to be increased, or the AUDIO signal be measured at TP13 instead of J6.



9 Packaging



Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 9 48-pin VQFN Mechanical Outline (Q3)

Order as part no. CMX7158Q3

About *FirmASIC*®

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

CML Microcircuits

United Kingdom	p: +44 (0) 1621 875500	e: sales@cmlmicro.com techsupport@cmlmicro.com
Singapore	p: +65 62888129	e: sg.sales@cmlmicro.com sg.techsupport@cmlmicro.com
United States	p: +1 336 744 5050 800 638 5577	e: us.sales@cmlmicro.com us.techsupport@cmlmicro.com

www.cmlmicro.com