Designing a 3.5GHz GaAs HBT Doherty PA MMIC

The Doherty Power Amplifier topology offers improved efficiency at back-off compared to conventional PAs, at the expense of added design complexity. Using a commercially-available GaAs HBT process, a Doherty PA capable of producing +38dBm of output power at 3.5GHz was designed and measured. The two-stage design was packaged in an 8x8mm QFN package, mounted onto an evaluation board (Figure 1) and good measured-to-modelled agreement was achieved.

Introduction

The Doherty Power Amplifier (DPA) topology offers a proven and reliable approach for improved efficiency when operating backed-off from compression. This white paper describes the design of a 3.5GHz GaAs Heterojunction Bipolar Transistor (HBT) Doherty Power Amplifier (DPA) MMIC. Such amplifiers are increasingly being deployed in 5G New Radio (NR) small cell applications for which GaAs HBT technology is particularly suited offering good efficiency (PAE), linearity and ruggedness as well as low cost.

Due to the high peak to average ratios (PARs) of 5G NR signals, power amplifiers in these applications are typically operated around 8dB or 9dB backed-off from saturation. The Doherty architecture allows for higher back-off efficiency compared to the conventional class AB architecture.

The use of digital pre-distortion (DPD) at high modulation bandwidths is also frequently used in these applications and the DPA presented here is well suited to operation with DPD, which allows the required modulation fidelity to be preserved.

Target Specification

An abridged requirements specification for the DPA is given in Table 1. The ACPR (Adjacent Channel Power Ratio) requirement is specified with and without correction. This refers to the use of DPD, which allows a significant improvement in ACPR at a given output power level.

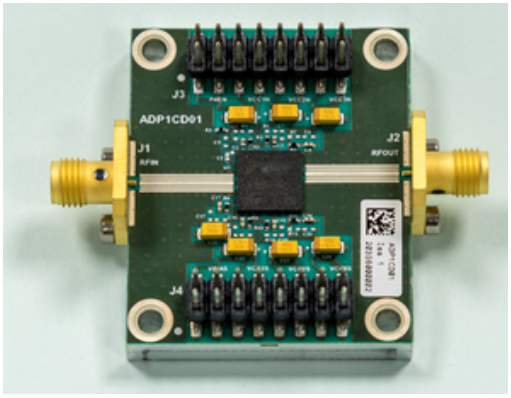

Figure 1: Packaged 3.5GHz HBT DPA MMIC on Evaluation Board

Block Diagram

A block diagram of the DPA is given in Figure 2. It consists of a Class AB input stage driving a two stage Doherty amplifier comprising a main amplifier and an auxiliary amplifier operating in parallel. In the Doherty architecture the auxiliary amplifier is "off" for lower input drive levels and the amplification is performed by the main amplifier. As signal levels increase the auxiliary amplifier starts to contribute to the amplifying process. It is only active when the signal levels are high and is dormant for low signal levels, allowing improved efficiency when amplifying complex modulated waveforms having high PARs. The signal from the Class AB input stage is split between the main and auxiliary amplifiers using a quadrature splitter so that the signal going to the main amplifier leads the signal to the auxiliary by 90°. In this implementation of the Doherty PA the main and auxiliary amplifiers are the same size, making this a symmetrical Doherty architecture.

Parameter	Units	Target Specification	Comment
Frequency Range	GHz	3.3 – 3.7	11.4% fractional bandwidth
Gain	dB	30	Small signal
		31	At 30dBm output power
Input Return Loss	dB	11	
Output Return Loss	dB	8	
Output Power	dBm	39	At 3dB gain compression, 10µs pulse width, 10% duty cycle
PAE	%	25	At 30dBm output power
ACPR (uncorrected)	dBc	-28	At 30dBm, NR 100MHz, PAR 8.5dB at 0.01% probability
ACPR (corrected)	dBc	-47	

Table 1: Target Specification

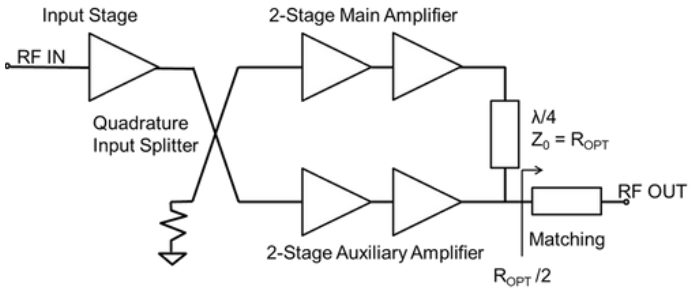

Figure 2: Block Diagram of a Doherty PA

The main amplifier is biased into class AB and the auxiliary amplifier is biased at a much lower current density approaching class B.

The outputs of the main and auxiliary amplifiers are combined using a Doherty output combiner consisting of an impedance inverter which is represented by a quarter wavelength transmission line and a matching network. The quarter wavelength line has characteristic impedance Ropt where Ropt is the optimum load resistance to present to both the main and auxiliary amplifier output stages for best power and efficiency at 3dB compression. The matching network transforms from 50Ω down to Ropt/2 at the combining point.

HBT Process Selection

Two GaAs HBT processes were considered for the DPA, a 5V HBT process and a 12V HBT process. Both processes are suitable for 5G small cell applications.

Compared to the 5V process, the 12V process has lower Ft and current gain but benefits from a higher DC supply voltage. This means that a small transistor unit cell size, implemented on the 12V process can operate at a higher power density than on the 5V process.

Higher power density can potentially lead to a smaller die area, however, when constructing power transistors on the 12V process it is advisable to implement these with a greater number of small but appropriately spaced unit cells for best thermal performance. This means the die area advantage over a multi-cell transistor of similar power capability implemented on the 5V process comprising of larger but fewer unit cells is not as significant as may be initially expected.

For a given power requirement, the optimum load resistance is higher and potentially easier to match to over a wider band (e.g. 25% fractional bandwidth) for the 12V process compared to the 5V process. However, the target fractional bandwidth 11.4% could also be adequately covered by the 5V process and the desirability of a lower supply rail resulted in the selection of the 5V process.

Unit Cell Selection and Ballasting Approach

Bipolar RF power transistors are implemented as an array of multiple unit cells, which allow the dissipated power to be more easily distributed. The trade-offs to consider when selecting the size of the unit cell for use within a multi-cell power transistor are thermal vs die area, and the amount of parasitic interconnect required to link the unit cells within the power transistor.

For a given emitter area operating at a given power density, a multi-cell power transistor comprising of a greater number of smaller unit cells will be better thermally as the heat is spread over a wider die area although this will require more interconnections. A multi-cell power transistor comprising of fewer unit cells will have less parasitic interconnections and be more compact but may be more prone to thermal issues.

The selected unit cell was a similar size to those used in commercial cellular HBT PA products and allows good thermal distribution across the multi-cell transistor.

Ballasting is essential in HBT power amplifiers to prevent thermal runaway and ensure even operation of the unit cells in a multi-cell power transistor. The two main ways of ballasting a unit cell are emitter ballasting where a smaller value resistor is placed in series with the emitter and base ballasting where a larger value resistor is placed in series with the base. Figure 3 shows the selected unit cell with base ballasting.

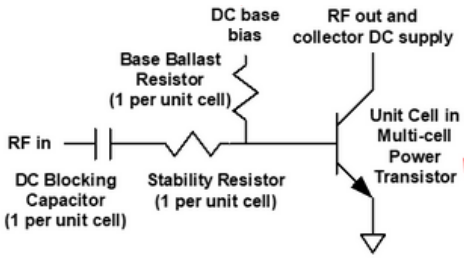

Figure 3: Unit Cell with Base Ballast Circuit

In this case the ballast circuit conveniently forms a bias tee at the input of the unit cell where the DC bias is applied to the top of the ballast resistor and the RF is applied at the input to the DC blocking capacitor. The circuit also includes a smaller value resistor in the RF path to ensure stability within the band of interest.

Unit Cell Performance

Figure 4 shows the Gmax and K-factor for the selected unit cell with ballast circuit in common emitter configuration biased at 5V at a class AB bias point. The bias current density is a trade-off of efficiency with gain and linearity. The unit cell simulation was biased using a voltage source applied at the top of the ballast resistor. In this configuration the unit cell is unconditionally stable from the bottom of the target band and has a maximum available gain of ~15dB at the top of the band. Figure 5 shows the large signal gain and PAE vs output power at 3.5GHz for the unit cell in the same configuration and class AB bias point but with optimised fundamental and harmonic termination impedances determined from load-pull simulations. In this case the unit cell achieves 24.3dBm output power and a corresponding PAE of around 80% at 3dB compression dropping to 28% at around 9dB BO. A modest degree of gain expansion is evident.

Determining Number of Unit Cells and Number of Stages

The simulated unit cell performance was used to determine the total number of unit cells that would be required in the combined main and auxiliary output stages of the DPA to meet the target output power, allowing for output losses and some margin.

The simulated unit cell gain when configured as described above, together with expected losses in gain due to the Doherty architecture and on-chip passive networks for matching, biasing, splitting and combining resulted in the selection of a 3-stage design.

Knowing the number of unit cells in the output stage, the number of unit cells in the other two stages can be determined. This is a trade-off between linearity and efficiency. A higher number of unit cells in the preceding stages, i.e. the main (and auxiliary) driver stage and the input stage, would give better linearity but lower efficiency.

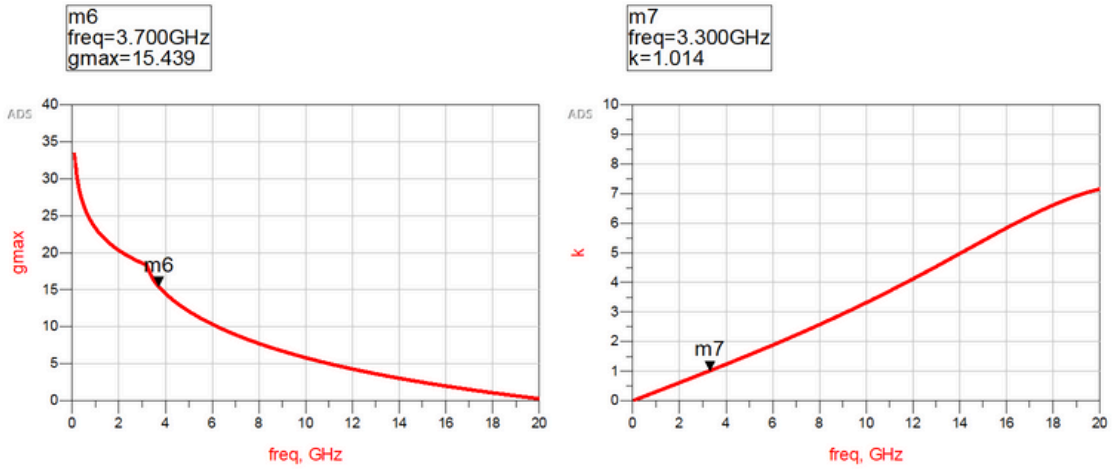

Figure 4: Gmax and K-factor for a Unit Cell with Base Ballast Circuit biased at 5V

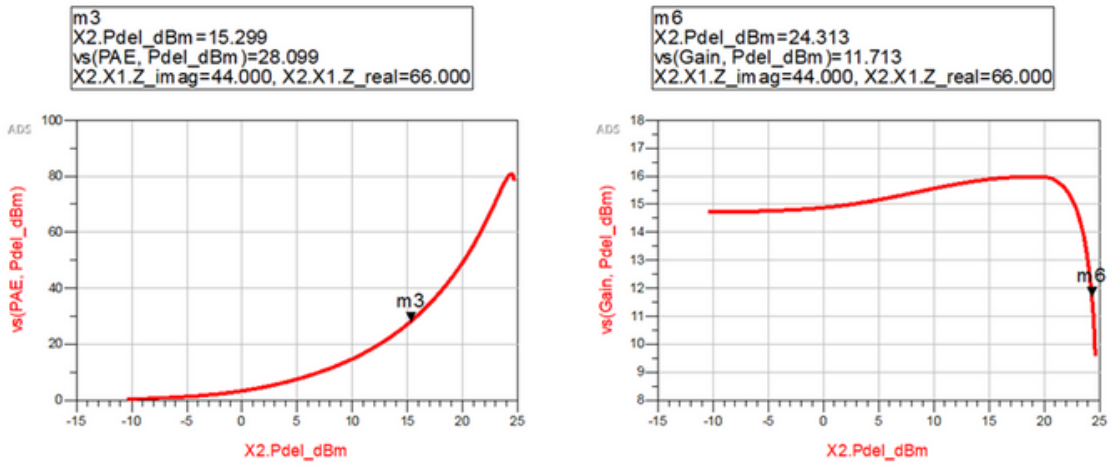

Figure 5: PAE and Gain vs Output Power for a Unit Cell with Base Ballast Circuit at 3.5GHz with Optimum Fundamental and Harmonic Terminations

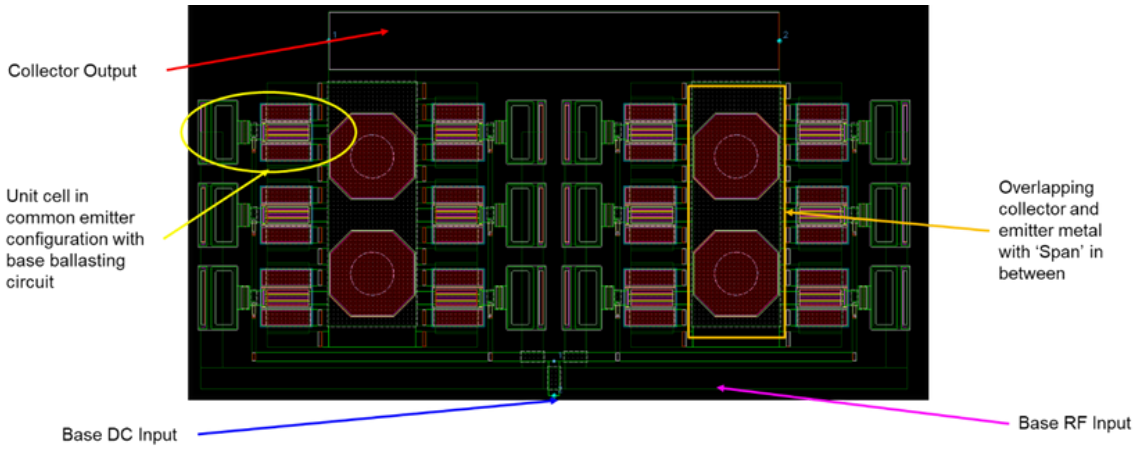

Figure 6: Example Layout of a Multi-Cell Power Transistor

Multi-cell Transistor Layout and Modelling

The unit cells in each of the main and auxiliary output stages were implemented as two parallel sets as this would allow the unit cells to be driven more evenly compared to a single set.

Figure 6 shows an example layout of a multi-cell transistor. The combined collector connection is at the top and the combined RF and DC base inputs are at the bottom. The UCs each with individual base ballast circuits are evident and the hexagonal structures are ground vias for the emitters (common emitter configuration). The combined collector and emitter metals overlap in a couple of areas and use of a relatively thick layer of dielectric with relatively low dielectric constant in between helps to minimise the associated collector to emitter parasitic capacitance.

The parasitics introduced in the multi-cell layout need to be accurately modelled so they can be accounted for in the design. This should be performed using EM simulation to obtain best accuracy.

Bias Circuit Design

When biasing PAs in deep class AB, the use of an emitter follower as a base current driver helps provide the rapidly increasing base bias current during the RF ramp-up.

Figure 7 shows a power transistor comprised of N parallel unit cells in common emitter configuration.

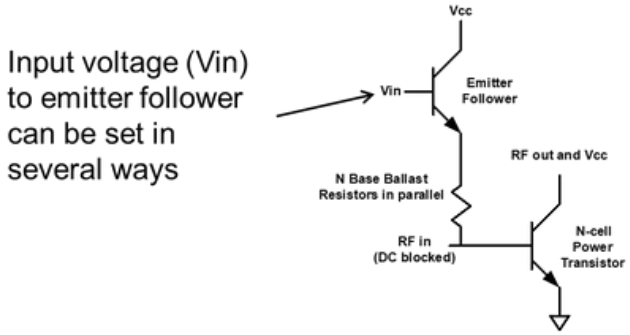

Figure 7: Emitter Follower in Base Bias Circuit

The collector is biased at Vcc, the base is biased through a DC ballast resistor equivalent to N unit cell ballast resistors in parallel. The top of the DC ballast resistor goes to a low impedance source provided by a smaller transistor in emitter follower configuration which is used to drive the base current to the power transistor.

The collector of the emitter follower can use the same supply as the power transistor collector. This is less critical to biasing of the power transistor than the input voltage (Vin) at the base of the emitter follower. This input voltage can be set in several ways. The approach adopted in the DPA was to use two stacked diodes biased through a resistor which provide temperature compensation for the PA transistor. The circuit was adapted for class AB bias for the main amplifier and near class B operation for the auxiliary amplifier. An enable function for the DPA was also included.

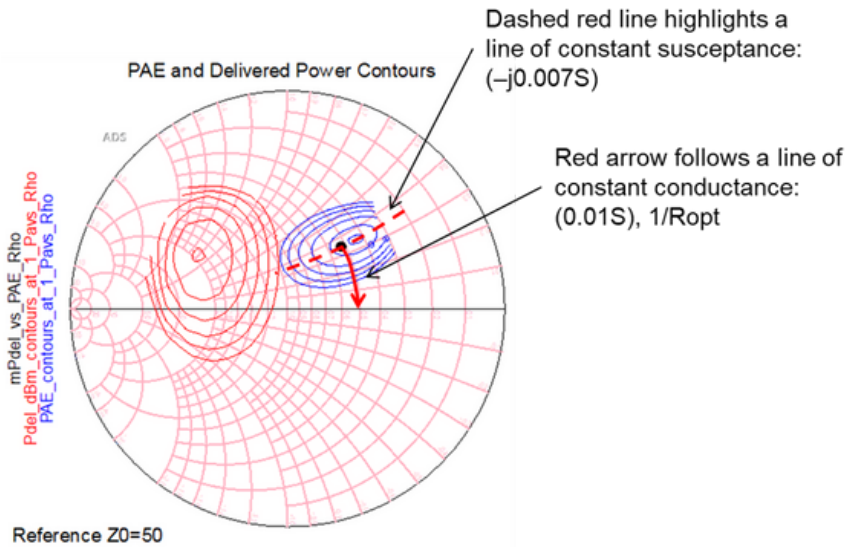

Figure 8: Load-Pull Data at 3.5GHz for a Single Unit Cell (Optimum Load Admittance, Yopt, Indicated by Black Dot)

Doherty Output Combiner Design

To design the Doherty output combiner, Ropt for the DPA must first be determined. This is normally done using load-pull simulation which was initially carried out on a single unit cell.

Figure 8 shows load-pull simulation data at 3.5GHz plotted on an admittance chart for the single unit cell (UC) with ballast circuit, as shown earlier in Figure 2. The UC is in common emitter configuration biased at 5V. The black dot in Figure 8 indicates the optimum fundamental load admittance, Yopt, for the single unit cell selected for good efficiency and adequate power - nearer the centre of the efficiency

contours (blue) than the power contours (red). The real part of Yopt is given by 1/Ropt and equal to 0.01S. Scaling this gives an Ropt of ~4Ω for the full DPA.

Implementing the impedance inverter in the Doherty output combiner as a quarter wavelength microstrip line of 4Ω characteristic impedance at 3.5GHz is impractical on an MMIC. The required width and length would take up an enormous amount of chip area and pose layout difficulties. Figure 9 shows a more practical implementation of the impedance inverter more suited to MMICs.

This uses a Tee equivalent although a Pi equivalent could also be used if it offered an advantage. One configuration may be selected over the other depending on the required harmonic terminations. The Tee equivalent is formed by two equal lines of higher characteristic impedance with a shunt capacitor in between.

The combined length of the two lines is overall shorter than a quarter wavelength and they are much narrower than a 4Ω line. With a shunt MIM capacitor in the middle, this approach is suitably compact for integration on to an MMIC and was adopted for the DPA.

The other key part of the Doherty output combiner is the matching network which presents Ropt/2 at the combining point or 2Ω in this case. The topology shown in Figure 8 is a two-section, low pass network and is like that selected for the DPA.

Band-pass and high-pass matching structures also offer their own set of advantages, but the low-pass network was chosen as it provides good harmonic rejection. Two sections were required to achieve the high transformation ratio (50Ω to 2Ω) over an adequately wide band. The DPA employed high impedance lines for the series matching inductors, shunt MIM capacitors and a series MIM capacitor at the RF output for DC blocking.

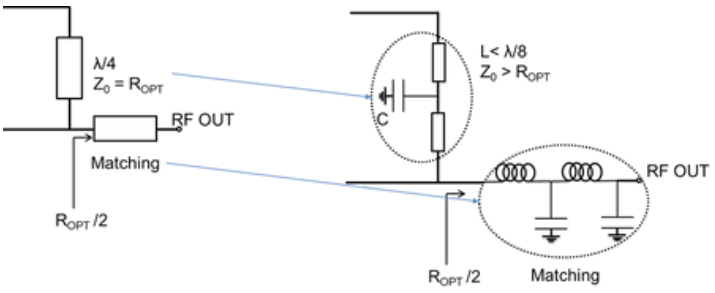

Figure 9: Implementing Doherty Output Combiner on an MMIC

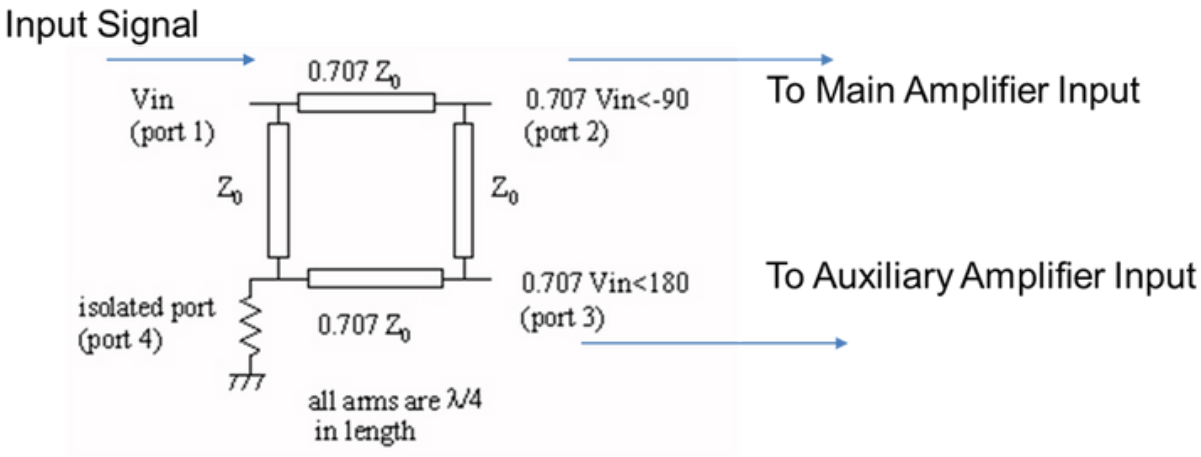

Figure 10: Branch Line Coupler for Input Splitter

Doherty 90° Splitter Design

The input signal to the main and auxiliary amplifiers is split in quadrature to compensate for the 90° phase shift of the impedance inverter in the output combiner. Typically, the input signal to the main leads the input signal to the auxiliary by 90°.

Figure 10 shows a branch-line coupler, a common way of doing this split. As depicted, this version of the coupler provides a nominally even amplitude split between the main and auxiliary amplifiers but versions with uneven splits can also be designed. Although the coupler as shown may be suitable for a PCB, the use of four quarter wavelength (λ/4) lines at 3.5GHz makes it prohibitively large for integration on an MMIC.

A more suitable implementation for MMICs is shown in Figure 11 where the λ/4 lines have been replaced with lumped Pi equivalents. This is similar to that implemented in the DPA MMIC which used spiral inductors, shunt MIM capacitors and an appropriately sized TFR for the 50Ω termination. Simulation results for an early version of this lumped branch-line coupler design are shown in Figure 12.

Final Schematic and Simulated Performance of the DPA

The final schematic of the DPA is shown in Figure 13. All key passive components use models derived from EM simulation including the output combiner and input splitter which both use look-a-like symbols. The 2-stage main and auxiliary amplifiers with corresponding bias circuits are indicated as well as the input stage.

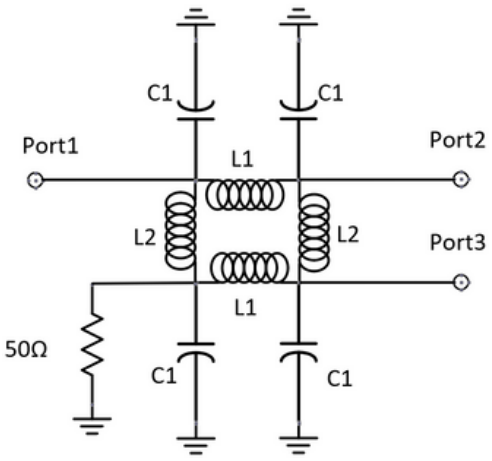

Figure 11: Lumped Element Implementation of a Branch-Line Coupler

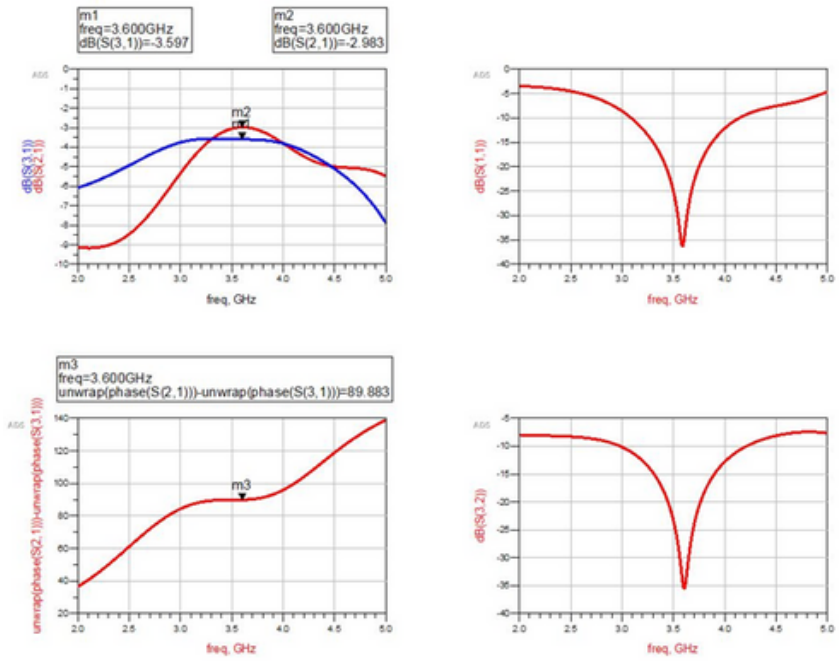

Figure 12: Simulation Results for Lumped Branch-Line Coupler

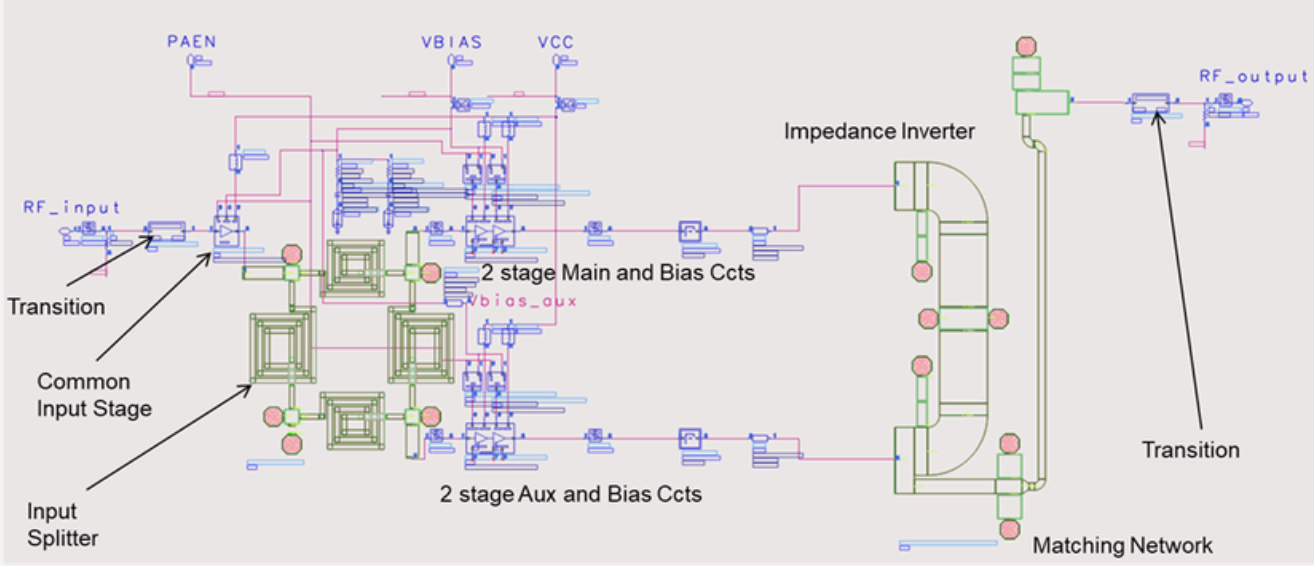

Figure 13: Top Level Schematic of 3.5GHz HBT DPA MMIC

Also included are package transition models as ultimately the part is to be housed in an SMT QFN package. Figure 14 shows a placement layout for the MMIC. Figure 15 shows the simulated small signal performance. The gain is ~26.5dB ±1dB across the band, the input return loss is better than 11dB across the band and the output return loss better than 10.5dB across the band.

The simulated performance compares well with the target specification.

Measured Performance

The fabricated MMICs were assembled into 8mm x 8mm QFN SMT packages and mounted onto evaluation PCBs as shown in Figure 1. A TRL calibration standard allowed measurements to be referenced to the package RF pins.

Several parts were tested, and all powered up to the expected quiescent current indicating that the bias circuits and enable function were working well and the design was thermally stable.

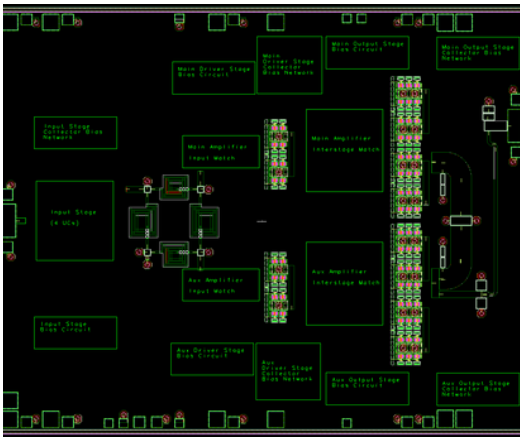

Figure 14: Placement Layout of 3.5GHz HBT DPA MMIC

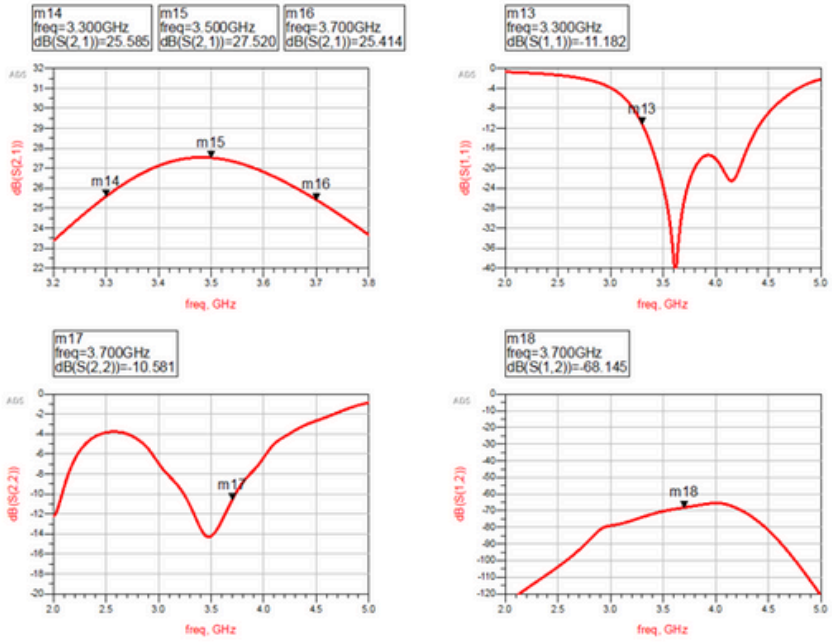

Figure 15: Small Signal Simulation Results of 3.5GHz HBT DPA MMIC

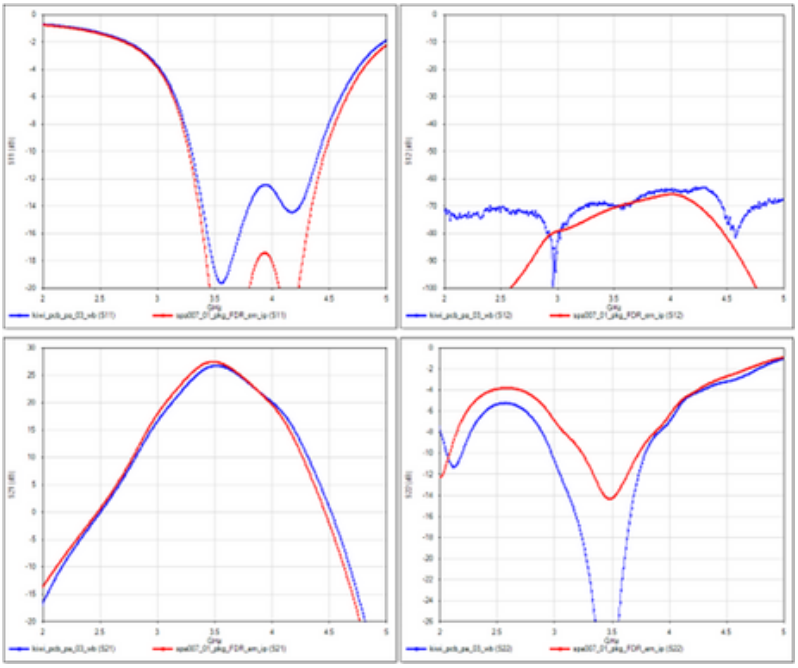

Figure 16: Measured and Modelled S-parameters

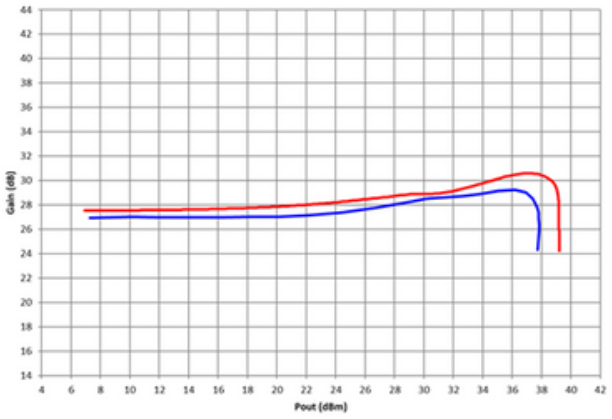

Figure 17: Measured and Modelled Gain vs Output Power at 3.5GHz

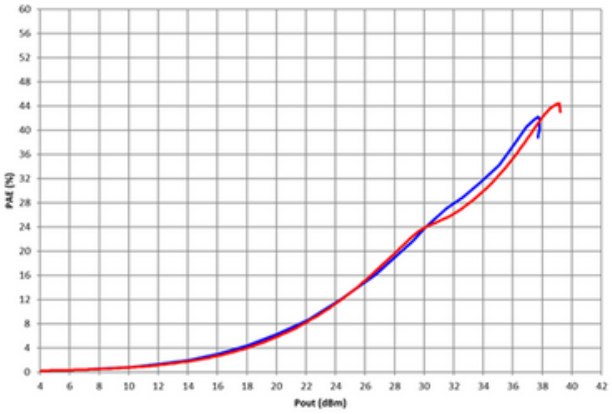

Figure 18: Measured and Modelled PAE vs Output Power at 3.5GHz

Figure 16 shows measured small signal S-parameters (blue traces) for a typical sample overlaid with the final simulated performance (red traces). The agreement in small signal gain is very good with the measured within 1dB of the simulated.

Figure 17 shows the measured and modelled gain versus output power at 3.5GHz.

Good agreement is evident with the measured output power around a dB lower than simulated.

Figure 18 shows the measured and modelled PAE versus output power at 3.5GHz. Again there is good agreement; the measured peak PAE is just ~2% points lower than the simulated and virtually the same at the 30dBm operating point.

ACPR testing with digital pre-distortion (DPD) was carried out using 5G NR-like waveforms. At an average output power of 30dBm, good performance was reported for modulation bandwidths up to 100MHz with a corresponding PAE of ~22%.

Conclusions

This white paper has described the design of a 3.5GHz GaAs Heterojunction Bipolar Transistor (HBT) Doherty Power Amplifier (DPA) MMIC designed on a 5V HBT process. The challenges of implementing this topology have been discussed. The first-pass design performed well against the target specification and showed good agreement with simulation.